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Research on Optimal Design of Chip ESD Protection Circuit Based on CMOS Technology

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Abstract. A high frequency circuit based on ESD protection and a new type of power grounding clamp circuit are designed. The oblique edge interfinger diode is used to achieve the optimal design of layout and performance. The design of electrostatic discharge protection circuit and flowsheet were completed in Jazz0.18-micron silicon germanium BiCMOS process. The protection voltage of electrostatic discharge is 3000 V. Higher electrostatic protection level can be obtained by changing the bifurcation index of diode. Improved protection of up to 4500 volts can be achieved. Through the test of the chip, it is proved that the chip fully meets the design requirements and can realize various types of digital circuits.

Keywords: CMOS; ESD; Full Chip ESD Protection; Analog to Time Conversion Chip.

1. Introduction

The continuous reduction of oxygen layer thickness and characteristic scale of CMOSIC gate leads to a significant decrease in the high voltage and high current performance of MOS transistors. Electrostatic discharge (ESD) effect is an important factor to improve the reliability of CMOSIC. More than 30% of the faults in the whole IC are caused by electrostatic interference, so the protection line and structure of electrostatic interference has become a key issue in the reliability design of IC. At present, the common ESD protection circuit structure and function are mainly based on grid grounding nMOS protection and thyristor protection [1]. However, they also have some problems, such as occupying too much chip area, anti-ESD voltage needs to be further improved. In order to overcome the defects of GG-nMOS protection, a new protection scheme is proposed based on the principle of full-chip electrostatic discharge protection, which can achieve the same aspect ratio as GG-nMOS without additional processing. The new ESD and GG-nMOS polynomial (MPW) streamers are performed using multiple silicon wafer (MPW) technology with the same width-to-length ratio of 50:1. The effect of the flow sheet is tested and compared [2]. Experimental results show that the GG-nMOS protection circuit with the same aspect ratio can improve its antistatic performance by about 32%, and occupy a smaller chip area and a smaller static current.

2. ESD Preventive Components

In the design of ESD protection circuit, appropriate components should be selected first to form the ESD discharge channel. Generally speaking, ESD protection devices need to have seven basic conditions: 1) to provide an efficient release channel for electrostatic charges. 2) This operation is not valid when the general input/output signal is passed. 3) Reduce the input capacitance and resistance. 4) Minimize the coverage area under the premise of ensuring robustness. 5) Strong resistance to linkage. 6) As far as possible do not add mask, do not repair the reform process and compatible with the general process. 7) It has strong pressure resistance. The first, second, and fifth are the most basic conditions. 3, 4 indicators basically meet the requirements, but because the area increases, the capacity of the capacitor also increases, so in the specific design process must be in the electrostatic discharge protection level and the overall performance of the device to make a certain balance. Under the general process conditions, the design of ESD can be fully satisfied, and under higher process conditions, due to the addition of self-aligned silicon materials in LDD, SAB, ESD, etc., often need to be added in the design of ESD. If the design is to comply with article 6, then only general equipment

can be used as ESD protection lines, if it is to comply with Article 7 then it is necessary to increase the production of SAB, ESD injection, or other high voltage equipment.

3. Circuit Design

GG-nMOS is the most widely used ESD protection circuit architecture in the industry today, as shown in Figure 1 for a typical GG-nMOS and parasitic npn tube diagram (image cited in Sustainability 2023, 15(13), 10126). Since the gate, source and substrate are all grounded, no conduction channel can be generated, so that the MOS transistor cannot be turned on. When a positive ESD pulse is added between the drain and the ground, the drain voltage will rise until the reverse biased drain/liner junction will cause an avalanche breakdown, at which time a large number of holes will flow from the drain to the substrate, causing the substrate potential to increase. When increased to a certain extent, the source/liner junction will be positively biased and the parasitic npn tube will open. GG-nMOS enters the negative difference region, when the drain to substrate voltage in the parasitic npn tube drops from the maximum value Vt1, the npn tube works in self-biased mode after reaching the maintenance voltage VSP, and most of the ESD current is maintained by the parasitic npn tube bipolar structure, that is, the Snapback conduction mode [3]. In this case, the electrostatic discharge flows through the substrate to the power side, and its driving capacity is much larger than the conductive capacity of the surface channel, until a second breakdown occurs. The I-V characteristic curve of TLP test of GG-nMOS under ESD loading is shown in Figure 2 (image cited in Electronics 2020, 9(5), 718).

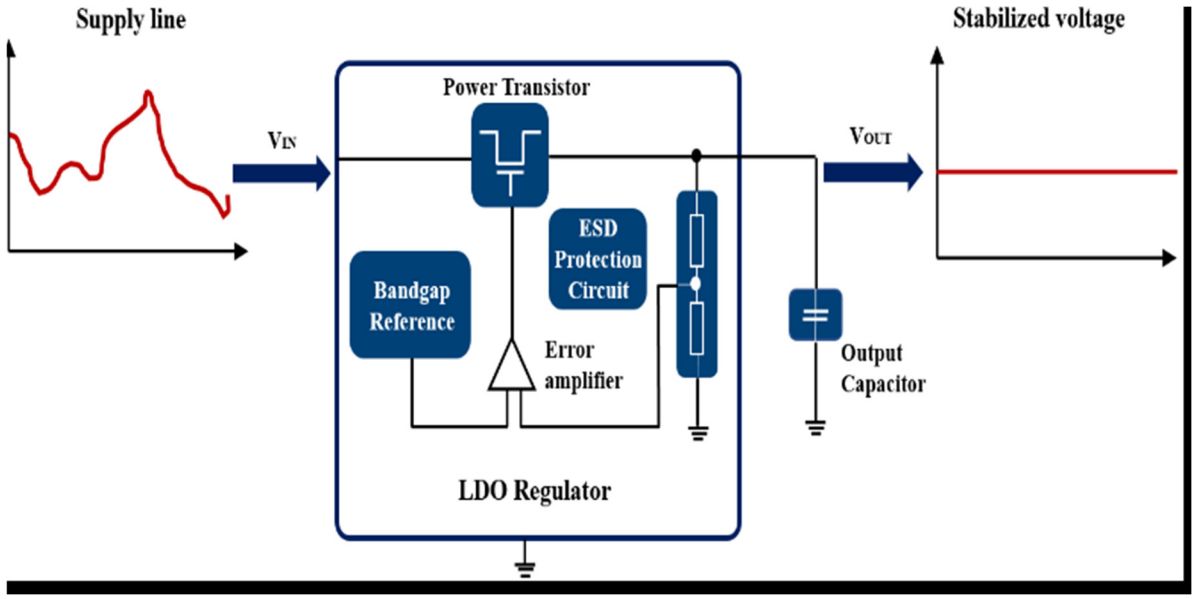

Fig 1. Schematic diagram of GG-NMOS and its parasitic npn tube

It can be seen from Figure 2 that in order to obtain better anti-ESD performance, it is generally necessary to reduce Vt1 and increase Vt2 to ensure that the protection circuit will not rise to damage its internal circuit before starting, and the most common Vt2 is to increase the tube, which is equivalent to multiple single-finger nMOS devices in parallel [4]. Because of the process, the on-voltage of each tube is different. Generally speaking, Vt1>Vt2, so there will often be a secondary breakdown in the conduction process of 2 to 3 tubes during ESD discharge, but the other tubes have not been opened, resulting in a significant reduction in the ability to resist ESD. If the Vt1 of the finger strip is <Vt2, then the voltage of the triggered finger strip is raised enough to trigger the other finger strips before the thermal breakdown, so that the finger strips can be opened one by one. In order to solve the problem of non-uniformity of GGnMOS conduction, it is generally solved by gate coupling, but this will not only increase the area of the chip, but also produce an independent capacitor on the drain end of the MOS tube, which makes the manufacturing process of the device more complicated.

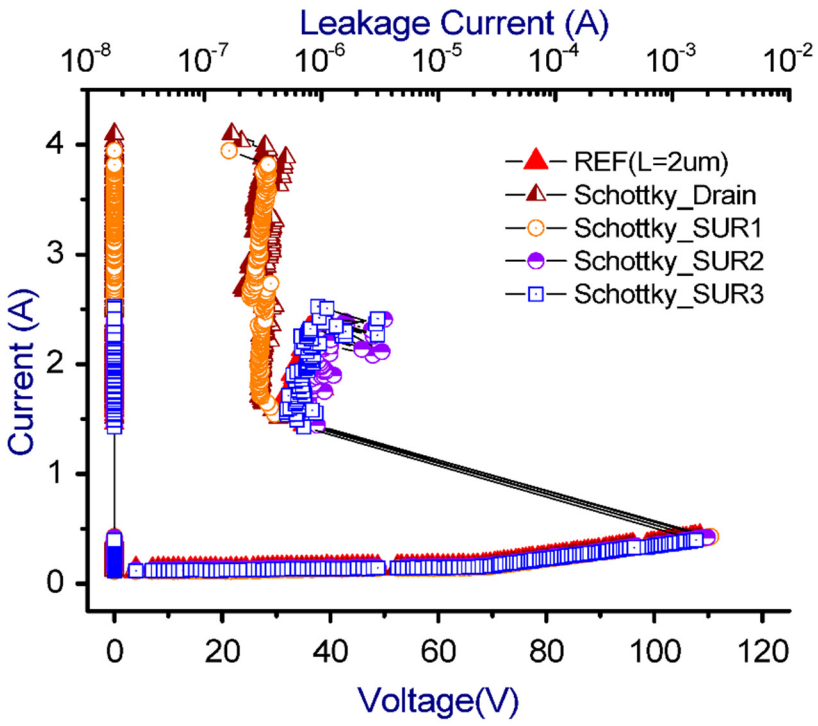

Fig 2. Typical TLP characteristic curve of GG-NMOS

4. Test and Analysis

The performance of the circuit is compared . The method based on GG-nMOS and ESD is proposed. And the MPW was streamed and packaged [5]. Two different types of protection lines are compared experimentally. A secondary breakdown occurred when the TLP tester had a maximum output current of 8 amps at a leakage current of 1 MA. The test results are shown in Figures 3 and 4.

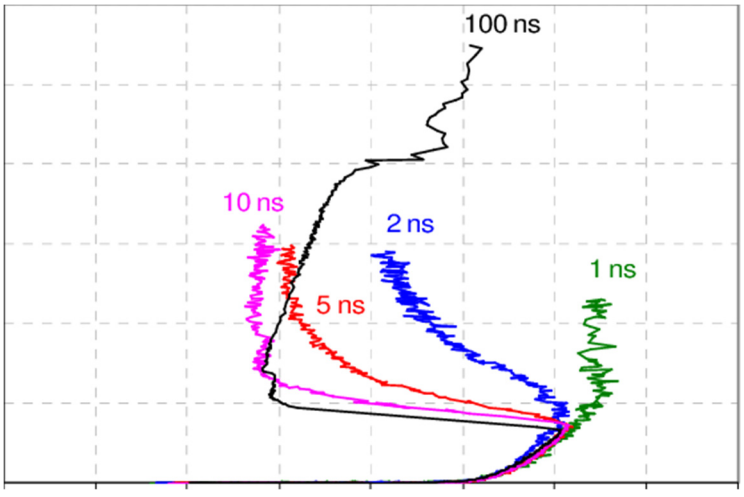

Fig 3. TLP characteristic curve of new structure

The results of a newly constructed ESD protection circuit, while FIG. 4 shows the TLP test results of a GG-nMOS that also has the same width ratio. It can be seen that the opening voltage Vt1 of this new structure ESD protection circuit is very low, far lower than the opening voltage of the conventional GG-nMOS protection circuit, while the Vt2 are much larger than the conventional GG-nMOS structure. The RON of the protection circuit of this new structure is larger than ON in the GG-nMOS protection circuit, and its advantage is that the slope of the I-V curve of the device from the maintenance voltage point to the secondary breakdown point is reduced, and the change of current with voltage is slowed down, which is conducive to the voltage exceeding Vt1 before reaching the secondary breakdown [6]. In addition, because there are two leakage channels in the structure, the

leakage current is relatively large when the voltage is the same. This is because the GG-nMOS protection circuit operates under the Snapback effect, so the leakage of GG-nMOS is independent of the channel length [7]. However, because the new structure proposed in this project has two leakage channels, and the large current mostly passes through the channel to achieve leakage, the Snapback effect is not significant, and its leakage mechanism is different from that of conventional GG-nMOS protection. In this paper, a kind of electrostatic discharge protection circuit which reduces Vt1 and increases Vt2 is developed to improve the antistatic performance.

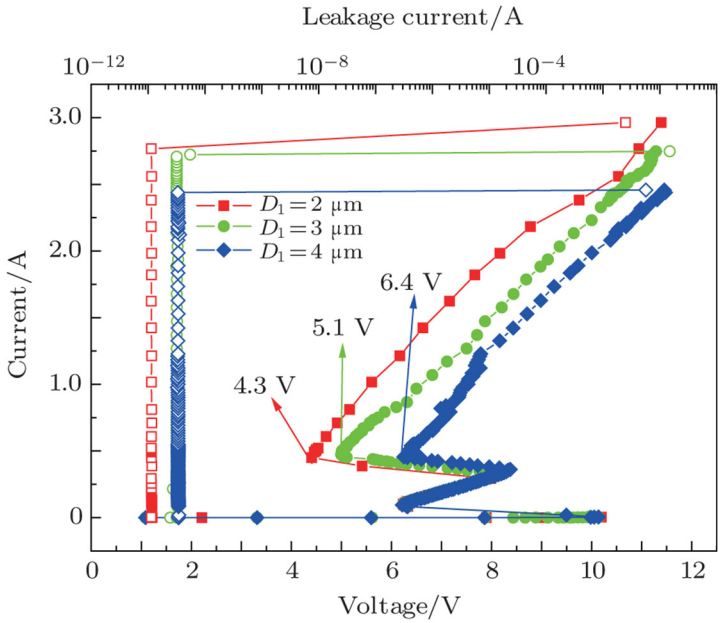

Fig 4. GG-nMOSTLP characteristic curve

5. Discuss

According to the above theoretical and experimental results, this phenomenon is closely related to the generation of impact ions. It is found that the backflush voltage of the element is closely related to the shape of the source, drain and substrate pn junction, the length of the channel and the bias voltage of the gate. The length of the channel and the bias of the gate in the process are the keys of ESD protection architecture [8]. In addition, during the discharge process, the smaller the channel length, the larger the electric field between the source-drain region, which is more conducive to collision ionization during the discharge process, and plays a better protective role for NMOS. The smaller the channel length, the larger the diode current can be obtained, and the discharge power can be released faster. However, because the width of the channel cannot be too small, there is already penetration between Si and Si before collision ionization [9]. Under the influence of electrostatic discharge, eutectic point will be generated between Si and Si, resulting in the failure of Si to work at low pressure. Normally, the channel length of the protective layer NMOS should be 1-3 microns. Considering that the lateral electric field is an important factor to induce and promote collision ionization, the NMOS gate is connected to the ground, so that the lateral electric field will not affect the bias on the NMOS gate.

The resistor serves to limit the current in the protective line. In addition, because of the action of the resistor, the voltage drop caused by the thin gate NMOS flyback of the resistor activates the thick gate NMOS field effect tube in the master protection circuit. N-type barriers operate in the normal state when they are in the ohmic characteristic region. In the process of electrostatic discharge, the N-trap resistor will produce high dynamic resistance in the saturation characteristic region, so as to limit the electrostatic discharge path, so as to protect the thin gate NMOS and the internal line. The basic principle of thick gate FMC protection is the same as that of thin gate FMC protection with ground grid. The essential difference between the two technologies is the difference in their starting voltage. In addition, when the electric field strength of the electric field tube is far away from the

wafer surface when it is swept back, the electric field strength changes with time. Therefore, in the case of not using laser diodes, field effect tubes are generally used as the main protection line. Aiming at the main shortcomings of the traditional LVTSCR, this project intends to use LVTSCR to replace the traditional thick gate structure field tube and improve its energy output efficiency in ESD. However, when using LVTSCR, its protection devices are often more complex.

6. Conclusion

The whole on-chip electrostatic discharge protection circuit is described in this paper. The performance requirement and selection principle of electrostatic discharge device are analyzed in detail. In this paper, different discharge states of electrostatic dampers are studied. Then the ESD protection circuit of the system is developed by using the XFAB0.6-micron CMOS process. The electrostatic discharge protection between the power supply and the ground wire is designed, and a certain amount of power clamp is set between the power supply and the ground wire. According to the US army standard mi-lstd-883, ESD entered 30 lines on the test chip. 30 lines can withstand electrostatic protection above 5 KV. At present, the main ESD protection technologies at home and abroad still include protection diodes, GG-nMOS and SCR. However, because ESD protection circuits are usually designed and developed according to special protection needs, there is no protection circuit that can be widely applied to various types of chips. The electrostatic discharge protection circuit developed by the author, which contains logic elements, can only be used for simple digital circuits, so its results will be further extended to RF, digital analog mixing and other aspects, is also the next step to do work. Compared with the conventional GGnMOS protection, the protection circuit not only has better antistatic property than the conventional GGnMOS protection, but also has weaker static property, which is consistent with the current low energy consumption design idea. In addition, the ESD protection circuit used in the scheme is completely consistent with the design idea of the conventional GG-nMOS, without adding other processes, and the chip area is reduced by 22% compared with the design idea of the same width and length ratio of GG-nMOS.

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