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The single inverter is affected by electromagnetic interference, and the protection mode

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Abstract. The easiest way to resist electromagnetic interference is to optimize the design to reduce interference. The electromagnetic interference received by a single inverter mainly comes from the influence of electromagnetic radiation on circuit topology and device type. Regarding circuit topology, it is recommended to adopt soft switching topologies such as active clamping flyback or LLC resonance, which can effectively reduce the voltage and current change rate in the switching process and reduce the switching noise by 6- 8 dB. In addition, multi-level technology can be introduced with 3-level or 5-level mating to control the output waveform THD to within 3%. In terms of changing the modulation strategy, such as using adaptive inverter PWM technology to adjust the switching frequency in real time to disperse harmonic energy, the switching loss can be reduced by about 30% with the dead time optimization algorithm. In terms of device selection, SiC MOSFETs with low gate charge (Qg<50nC) and low reverse recovery charge (Qrr<100nC) should be selected because their switching speed is more than 3 times faster than traditional silicon devices, which can significantly reduce high-frequency noise and thus reduce the impact. The PCB design must adopt a six-layer board stacking structure, including two complete power and ground planes. The key signal lines should be routed in strip wires, and the line widths should be accurately calculated according to the characteristic impedance requirements. In addition, the power loop layout should follow the principle of "shortest path", so that the area of the high-frequency current loop is less than 2cm², and low-inductance chip capacitors (such as 0402 package, capacitance 1nF) should be arranged between the drain-source of the MOSFET to absorb voltage spikes.

Keywords: Single inverter, electromagnetic interference, Design optimization.

1. Introduction

A single inverter is a power electronic device that converts direct current (DC) into single-phase alternating current (AC), usually with an output of standard civil voltage such as 220V/50Hz or 110V/60Hz, suitable for household, small commercial or single-phase load scenarios, its core function is to convert direct current (DC to AC) provided by solar panels and batteries. There are three types: Grid-tie, Off-grid, and Hybrid, which are used as outputs to modify the wave to achieve the purpose of grid connection [1,2] This has played a decisive role in integrating local photovoltaic power generation into the unified power grid. However, it will be affected by external electromagnetic influences during operation, resulting in reduced efficiency and signal distortion. Although the scope of action of a single inverter is often limited to the civilian field, with the popularization of photovoltaic power generation, its role has begun to appear.

Solving or mitigating this problem (e.g., devising a compensation method to reduce harmonic interference) is necessary to ensure its efficiency and signal authenticity. Below, we will describe how individual inverters are subject to complex electromagnetic influences, including internal and external electromagnetic interference. Providing adequate protection measures to ensure the operation's stability and authenticity includes improving the design idea and optimizing the user experience conditions. It also explains its impact as a source of interference.

2. Effect of Complex Electromagnetic Phenomena on Single Inverters

The emergence of complex electromagnetic phenomena is often generated and increased in the development of society. This problem's analysis helps us understand its impact on individual inverters [2].

The impact of the complex electromagnetic environment on single inverters is mainly reflected in several interrelated aspects. First of all, the electromagnetic interference (EMI) generated by high-frequency switching will affect the system through both conduction and radiation, which may not only cause the malfunction of the inverter's control circuit, but also interfere with the regular operation of the surrounding sensitive electronic equipment, which is caused by the interference may be coupled to the adjacent sensitive circuit. In addition, because the single inverter is the adjustment of the waveform, due to the influence of the complex electromagnetic environment on the harmonic characteristics, which leads to the change of its working stability, such as the high-order harmonics introduced by the PWM modulation process will lead to the distortion of the output voltage and current waveform, which not only increases the system loss, reduces the conversion efficiency, but also may cause grid compatibility problems and affect the regular operation of other connected equipment [3]. Of course, the voltage sag and surge impact caused by transient disturbances on the grid or load side will directly affect the stability of the DC bus voltage, and it is also an essential factor for the impact of a single inverter, because it directly affects the wave frequency and stability of the power grid. In severe cases, it may lead to overvoltage breakdown of power devices or system protective shutdown [4,5].

In high-frequency power electronic circuits, the influence of parasitic parameters on circuit losses is particularly significant. Specifically, a resonant loop consisting of parasitic inductance (Lp) and parasitic capacitance (Cp) produces a severe ringing effect, which can cause a double adverse impact: first, the oscillation tip of the voltage and current significantly increases the switching loss (measured data show that ringing can increase the energy loss of a single switching cycle by 30%-50%) [6,7]; Second, the resulting overvoltage stresses (e.g., MOSFET drain voltage spikes of up to 1.5-2 times the rated value) directly threaten the long-term reliability of the power device. This vicious cycle is further exacerbated at high frequency (fsw>500kHz) as the sensitivity of parasitic parameters to dv/dt and di/dt increases exponentially as the frequency increases, ultimately leading to a chain reaction of reduced system efficiency and shortened device lifetime. This is derived from the switching loss model with parasitic parameters, where the power dissipation per cycle is dominated by the resonant energy in Lp and Coss:

$$P_{\text{loss}} = \frac{1}{2} f_{\text{sw}} \left(C_{\text{oss}} V_{\text{peak}}^2 + L_p I_{\text{ring}}^2 \right) \tag{1}$$

where fsw is the switching frequency (Hz), which reflects the frequency of switching actions; Coss is the MOSFET output capacitance (F); Vpeak represents the peak voltage of the switching node (V), and Lp is the parasitic inductance of the loop (H); Iring stands for Peak Resonant Current (A)

At the same time, the electromagnetic coupling between the high and low voltage circuits inside the system may lead to distortion of the control signal, which in turn affects the accuracy of the PWM drive and even serious failures. In terms of thermal effects, eddy current losses and switching losses caused by high-frequency operation will significantly increase the operating temperature of key components, and excessive temperature rise will not only accelerate the aging of components but also may change the characteristic parameters of magnetic components, further affecting the overall performance of the system.

The influence of electromagnetic radiation generated by itself is reflected in the circuit operation, and the electromagnetic interference generated by high-frequency switching action will react to the inverter itself through conduction and radiation. The arrival of interference is coupled to the control circuit through the power supply line and ground circuit, causing the PWM drive signal to be distorted or jitter, which may cause a straight-through short circuit between the upper and lower bridge arms. Radiated interference will form a complex electromagnetic field distribution inside the chassis,

interfering with the regular operation of the voltage and current sensing circuit and distorting the output waveform. This self-interference phenomenon is often more apparent when the inverter works in a light-load or no-load state. The high-frequency ringing and voltage spikes generated during switching directly affect the power MOSFET or IGBT [3]. Electromagnetic interference can also cause delay or distortion in the gate drive signal, increasing switching losses and decreasing system efficiency. In a strong interference environment, the conversion efficiency of the inverter may be reduced by 3-5 percentage points. High-frequency interfering currents are coupled to the heat sink through parasitic capacitance, which can cause abnormal heating.

3. How to Upgrade a Single Inverter to Avoid Interference

3.1. Design optimization

The easiest way to resist electromagnetic interference is to optimize the design to reduce interference [8]. The electromagnetic interference received by single inverters mainly comes from the influence of electromagnetic radiation on circuit topology and device type. In terms of circuit topology, it is recommended to adopt soft switching topologies such as active clamping flyback or LLC resonance, which can effectively reduce the voltage and current change rate in the switching process, and can reduce the switching noise by 6-8dB [9,10]. Its principle is that the active clamping flyback converter constructs a leakage inductance energy recovery path by introducing a clamping switch and capacitors, and realizes the main switch's zero-voltage turn-on (ZVS). This technology reduces the dv/dt during the switching process from 10V/ns to 3V/ns in the traditional flyback, effectively suppresses high-frequency ringing, and reduces conducted EMI by 6-8dB in the 1-30MHz frequency band. The LLC resonant converter uses the filtering characteristics of the resonator (Lr Cr) to make the switching waveform sinusoidal, and its harmonic amplitude is rapidly attenuated according to the law of $1/f^3$(The harmonic attenuation characteristics of LLC resonant converter are mainly determined by the resonant cavity parameters (resonant inductance Lr and resonant capacitance Cr), and its core mechanism is the second-order filtering characteristics at the resonant frequency $f_r = 1/2\pi\sqrt{L_r C_r}$.), and the radiated noise can be reduced by 10-15dB in the frequency band above 30MHz. Both topologies lessen the intensity of electromagnetic interference sources by extending the switching transition time (100-200ns), and with the optimized PCB layout (resonant loop area <5cm²), the measured EMI test margin of the whole machine can be increased by 8-10dB, which is especially suitable for demanding high-frequency power supply designs, such as 5G base station power supplies and new energy vehicle on-board chargers [11].

In addition, multi-level technology can be introduced with 3-level or 5-level mating to control the output waveform THD to within 3%. The core mechanism of multilevel technology is to reduce the voltage jump (dv/dt) to 1/(N-1) of the traditional two-level by increasing the number of output levels, and at the same time using the switching angle optimization control to cancel each other out of specific subharmonic components in the Fourier series expansion**. Taking the three-level as an example, by accurately calculating the switching angles θ_1 and θ_2, $\cos(5\theta_1)\cos(5\theta_2)=0$, the 5th harmonic can be directly eliminated. The increase of the number of levels will also concentrate the harmonic energy in the high frequency band of nfsw±mf0 (n,m is an integer), so that the THD in the low frequency band decreases according to the law of $1/N^2$, and finally achieves the goal of <3% THD. This effect is mathematically manifested as the filtering effect of the $\sin(n\pi/N)$ term of the Fourier coefficient, and when N≥3, the amplitude of the major lower harmonic will decay to less than 1/3 of the two-level scheme. For Multi-level output voltage expression and N-level inverters, the phase voltage Fourier expansion is as

$$V_{out}(\theta) = \sum_{k=1}^{N} V_{dc} \cdot \operatorname{sgn}(\sin\theta - \theta_k) \quad (2)$$

where N is the level (odd) and Vdc is the DC bus voltage(V); θk represents the k-th switching angle (rad); The symbolic function SGN compares the sinusoidal reference wave to the switching angle to generate a discrete level-switching signal.

$$V_{out}(\theta) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} [\sum_{k=1}^{N} \cos(n\theta_k)] \sin(n\theta) \quad (3)$$

They transform a traditional two-level ±Vdc output into multiple discrete voltage levels, bringing the output waveform closer to that of a sine wave. The next step is to precisely control the switching time of each level through harmonic cancellation, so that the phases of specific harmonics cancel each other. This requires the use of a system of harmonic cancellation equations.

$\sum_{k=1}^{(N-1)/2} \cos(m\theta_k) = 0$ The harmonic cancellation equation eliminates the corresponding harmonic components in the output waveform by precisely controlling the switching angle (θk) so that the sum of the cosine components of a particular harmonic order (m) is zero. The core mechanism is to use the symmetry and phase cancellation characteristics of the cosine term in the Fourier series to achieve selective harmonic cancellation by optimizing the combination of multiple switching angles (usually requiring numerical solution of nonlinear equations). For (N) level inverters, up to ((N-3)/2) harmonics of a specified number of times (e.g., 5th, 7th, etc.) can be eliminated, and the THD of the output waveform can be controlled to less than 3%. This method has important application value in photovoltaic inverters and industrial motor drives, which can significantly reduce the volume and cost of filters. Eventually, harmonic energy will be concentrated in the high frequency band, which can be more easily eliminated with filters.

In terms of changing the modulation strategy, such as using adaptive inverter PWM technology to adjust the switching frequency in real time to disperse harmonic energy, the switching loss can be reduced by about 30% with the dead time optimization algorithm [12]. In terms of device selection, SiC MOSFETs with low gate charge (Qg<50nC) and low reverse recovery charge (Qrr<100nC) should be selected because their switching speed is more than 3 times faster than traditional silicon devices, which can significantly reduce high-frequency noise and thus reduce the impact. The PCB design must adopt a six-layer board stacking structure, including two complete power and ground planes. The key signal lines should be routed in strip wires, and the line widths should be accurately calculated according to the characteristic impedance requirements [13,14]. In addition, the power loop layout should follow the principle of "shortest path", so that the area of the high-frequency current loop is less than 2cm², and low-inductance chip capacitors (such as 0402 package, capacitance 1nF) should be arranged between the drain-source of the MOSFET to absorb voltage spikes.

3.2. External structure

Physical protection is equally essential, and building a complete multi-level electromagnetic shielding system will help maintain efficiency and signal accuracy. To eliminate external interference as much as possible and keep the appropriate cost, the chassis should be made of a 1.5 mm-thick galvanized steel sheet, and all joints should be sealed with conductive rubber liners to ensure that the shielding effectiveness of the entire chassis reaches more than 60 dB. In addition, an additional mu-metal shield with high permeability can be added for particularly sensitive control circuit areas to reduce local magnetic field interference by more than 20 dB. All input and output cables must adopt a double-layer shielding structure, the inner layer is aluminum foil shielding, the outer layer is copper mesh braided shielding, and a 360-degree ring connection method is used to ensure the shield layer is reliably grounded [14].

A combined EMI filter is installed at the AC input and output terminals, and its insertion loss at the 1 MHz frequency point is required to be greater than 40dB, which is the protection of the port. The DC side is equipped with a composite protection circuit consisting of a gas discharge tube and a TVS diode to ensure that it can withstand the surge impact of 6kV/3kA. All signal ports must be equipped with ESD protection devices, and TVS diode arrays with response times of less than 1ns are selected. The grounding system adopts a three-level architecture design: the power ground, the shield ground, and the signal ground are routed separately, and finally, the grounding resistance should be controlled below 0.1Ω at one point. For particularly harsh industrial environments, consider adding a ferrite ring

to the outside of the chassis to absorb high-frequency interference, which will help reduce the interference from electromagnetic radiation [5,15].

4. Conclusion

This paper summarizes and analyzes the impact of electromagnetic interference generated by a single inverter in a complex electromagnetic environment. It also adds the possible implications of its electromagnetic changes on the overall components. Combined with the usual methods of reducing its interference (improving its structure and external protection). Single inverters are widely used in new energy power generation, aerospace, and industrial automation, but their stable operation in complex electromagnetic environments faces severe challenges. High-frequency switching noise and external electromagnetic interference lead to output waveform distortion, efficiency degradation, and control signal instability. The current research mainly focuses on hardware optimization and software control to improve the anti-interference performance. With the development of wide bandgap semiconductors, AI-assisted noise suppression, and new topologies, the reliability of inverters in extreme electromagnetic environments will further increase, and the same industrial demand will increase. This analysis of the related problems and solutions of individual inverters in the electromagnetic environment will help to improve and upgrade individual inverters.

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