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Research and Applications of EUV Lithography in Silicon Photonics

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Abstract. Extreme Ultraviolet (EUV) lithography is a photolithography technology used mainly in semiconductor manufacturing, especially for advanced nodes at and below 5nm. This technology holds promise for future adoption in photonic integrated circuits like silicon photonics, due to its superior resolution, overlay accuracy, and higher throughput than the current Deep ultraviolet (DUV) lithography method. While the EUV lithography system theoretically can improve the performance of silicon photonic devices such as waveguides, modulators, and photodetectors, EUV's current use in silicon photonics is limited due to high equipment costs and several technical challenges, including material and mask compatibility, photoresist development, and patterning. This article systematically analyzes the technical principles of EUV lithography, including the principle of the light source and the steps of the photolithographic process. Meanwhile, this article looks forward to the potential of applying EUV lithography in the future of high-density silicon photonic circuits integration. It discusses the core issues of EUV-based silicon photonics fabrication. Addressing these challenges will pave the way for higher volume production, help integrate the electronic and silicon photonic ecosystem, and provide a technical reference for the development of the next generation of silicon photonics technology.

Keywords: EUV; Silicon Photonics; Photoresist; Photonic Integrated Circuit.

1. Introduction

As the core of semiconductor manufacturing is photolithography technology, which accurately transfers circuit patterns to silicon wafers or various substrate materials to realize nanometer-level structures [1]. Photolithography is the key enabler of the fabrication of high-density integrated circuits, bringing greater performance and throughput while lowering the overall cost.

Extreme Ultraviolet (EUV) lithography is a photolithographic process using 13.5 nm wavelength light to create tiny features (down to 3 nm) on semiconductor wafers [2]. EUV lithography offers superior resolution and accuracy over previous 193 nm and 248 nm wavelength Deep ultraviolet (DUV) lithography processes, but currently is only used for cutting-edge traditional semiconductors [1]. Most of today's silicon photonic devices are manufactured based on the DUV lithography method, as current DUV equipment availability allows higher volume production, and the maturity of this technology enables a wider range of silicon photonic designs. Silicon photonics, the emerging field of silicon-based devices that focus on utilizing photons instead of electrons, has various telecommunication, integrated laser, LIDAR, and VLSI (very-large-scale-integration) applications [3]. The purpose of this research is to examine the current stage of development of these fields and the technical challenges of applying the EUV lithography process to silicon photonics fabrication.

The article illustrates the fundamentals of the EUV lithography process to further discuss how the application of EUV can pave the way to next-generation silicon photonic devices. The article also analyzes several technical challenges in integrating an EUV lithography system for silicon photonics manufacture.

2. Fundamentals of EUV Lithography Technology

EUV lithography is a photolithographic process that utilizes extreme ultraviolet light to pattern intricate features onto silicon wafers. It was proposed to reduce the complexity of DUV lithography and have finer resolution, capable of creating features below 4 nm [2]. Chip manufacturers typically use the wavelength of 13.5 nm light generated by a laser produced tin plasma, which is driven by 10.6 μm CO_2 gas lasers [4]. A multilayer mirror system focuses the light from the photomask onto the wafer, which reduces the pattern size by 4 times [5]. In addition, a series of manufacturing procedures are used to create the chip's minuscule patterns, which include photoresist application, mask alignment, exposure, and wafer development… The EUV-based fabrication process is responsible for producing advanced node semiconductors like high-performance logic chips and memory chips.

2.1. EUV Light Source

The EUV light source is typically generated in a vacuum chamber using the laser-produced tin plasma method, as Figure 1 shows**.**

First, a droplet of molten tin is generated at a rate of 50,000 times per second, falling into a collector below, each about 25 micrometers in diameter. These droplets are launched into the vacuum chamber at a rate of around 70 meters per second, where the lack of air inhibits the absorption of EUV radiation [6].

The tin plasma that produces extreme ultraviolet light is generated by a separate CO_2 laser system, usually placed directly below the floor under the EUV scanner system. The CO_2 laser is generated by applying an electric discharge to a gas mixture composed of carbon dioxide, nitrogen, and helium. The CO_2 drive laser can deliver a range of power from 10 W to 250 W.

Second, a low-intensity CO_2 laser pre-pulse strikes each tin droplet precisely as it falls, which flattens the droplet into a dish-like shape, preparing it for efficient vaporization. Then, a high-intensity main laser pulse hits the flattened droplet, vaporizing the droplet into a plasma that reaches a temperature around 220,000 °C [7].

The ionized tin plasma emits light at the wavelength of 13.5 nm, which is then passed into the scanner. Inside the scanner, a specialized multilayer mirror system reflects and collects the extreme ultraviolet light onto a precisely controlled wafer tray during chip patterning. The EUV light generation process is repeated at a rate of 50,000 times per second. Unlike the DUV process, which utilizes lenses to control the amount of light that passes onto the wafer, EUV chooses mirrors since all lens materials absorb light at 13.5 nm wavelength.

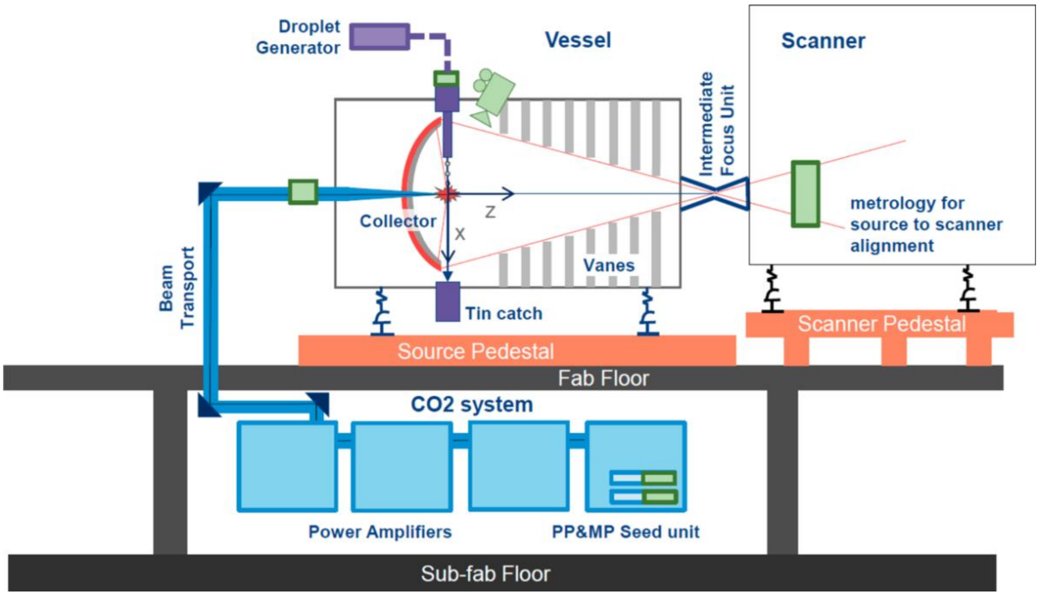

Fig. 1 Architecture of EUV source system [2]

The EUV light source generation process is illustrated above. The 13.5 nm EUV light finally hits the photomask controlled by an overlay alignment and control system. The overlay control system determines the accuracy of the EUV patterning process.

2.2. EUV Lithography Process

First, the silicon wafer is thoroughly cleaned to get rid of the impurities that can interfere with the later process. One of those cleaning methods is RCA clean. During RCA clean, a chemical mixture is used to first remove organic contaminants and then metallic contaminants, before rinsing and drying.

Next, a photosensitive polymer substance, photoresist, is uniformly applied to the silicon wafer. This material reacts to light of a particular wavelength, which the photochemical process forms the desired patterns along the path of the light.

In addition, a photomask or reticle that contains the circuit blueprint is then aligned over the wafer [8]. The Fig. 2 below illustrates the important steps in EUV lithography: wafer cleaning, photoresist application, EUV exposure, and other wafer developments like baking.

Extreme ultraviolet light laser passes through the transparent regions of the mask, exposing the photoresist. The light causes a chemical change, making the exposed areas either soluble or insoluble in a developer solution, depending on whether a positive or negative resist is used.

The wafer undergoes development where the exposed or unexposed photoresist is removed, and subsequent processes like etching, chemical vapor deposition, or ion implantation are used to form the final chip structure.

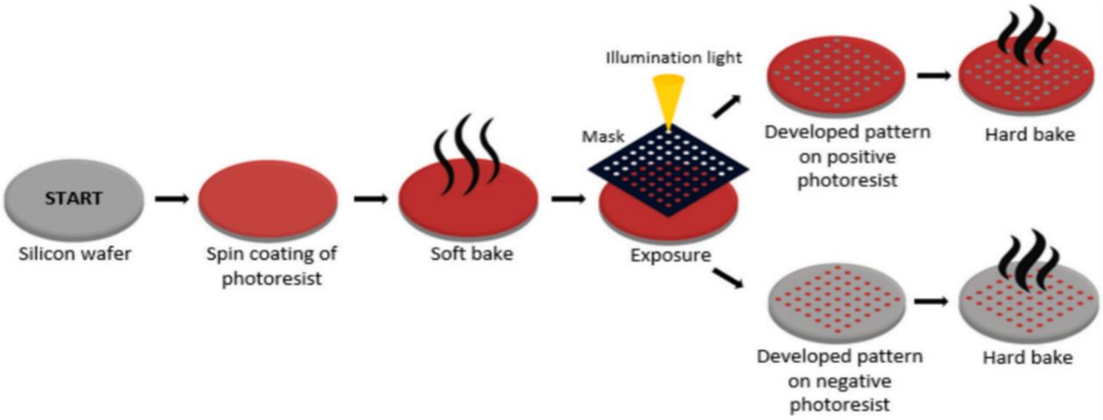

Fig. 2 EUV lithography process [9]

3. EUV Applications in Silicon Photonic Devices

EUV lithography’s higher resolution, tighter overlay control, and higher throughput hold the promise in silicon photonics applications. For example, EUV is capable of producing finer waveguides, more compact modulators, and ultra-dense PICs than the 193 nm DUV lithography process allows.

Silicon photonics is a photonic integrated circuit based on silicon as an optical medium. Photonic integrated circuit, like silicon photonics, has the advantages of low interconnect latency, large bandwidth, free of electromagnetic interferences, nonlinear design, and low power consumption [10]. Therefore, silicon photonics is considered to have great potential in optical communication-related applications such as data centers. Among all photonic integrated circuits, silicon photonics is considered the most promising due to its CMOS and existing fabrication compatibility. Compared with conventional chips’ bulk silicon wafers, silicon photonics utilizes silicon on insulator (SOI), which helps reduce the loss of optical signal. While being more compatible with electronic semiconductors than traditional optics, silicon photonics delivers better performance at the same cost as an electronic chip.

A typical silicon photonic chip has both electrical and optical supplies. A DC optical supply is needed since silicon is an indirect bandgap semiconductor that is not suitable for directly generating photons inside the material. Silicon photonics' high bandwidth characteristic can also be applied in AI data center communication, which needs to handle the enormous amount of traffic.

Currently, the majority of silicon photonic circuits are fabricated using a DUV light source at a wavelength of 193 nm or 248 nm. DUV lithography and fabrication process resemble the EUV system, while using ArF or KrF excimer laser [11, 12]. Moving from DUV to EUV lithography enables finer features to be created on the wafer, reduces the processing time, which increases production, and offers higher energy efficiency. Furthermore, EUV's higher resolution can reduce the reliance on the later multi-patterning process by having a single exposure instead of multi-patterning, which is a major challenge of existing silicon photonics fabrication.

3.1. Waveguides

First, silicon photonic waveguides define light paths and benefit directly from tighter lithographic control. EUV's 13.5 nm light can create narrower and more precisely defined waveguide cores and claddings than 193 nm tools, which improves mode confinement and allows denser routing.

Patterning periodic arrays of holes or slits with pitches pattern less than 100 nm is extremely challenging with 193 nm DUV process since it is below the wavelength of deep ultraviolet light. EUV's higher resolution enables producing these sub-193nm features, enabling novel couplers and dispersion-engineered waveguides. This also allows EUV to print fine slot dimensions with high fidelity, improving the overlap of optical and electrical fields and enhancing device performance [13].

Silicon photonic circuits require smooth curved bends to minimize scattering loss. EUVs' increased depth of focus can help maintain accurate curved shapes over the wafer. Using the lithography simulation and calibration (OPC) technique, EUV-based fabrication processes can produce ultra-dense grating couplers or photonic crystal sections that control dispersion and couplings more precisely.

3.2. Modulators

EUV lithography also improves optical modulators by enabling finer electrode and waveguide patterning. Silicon modulators generally rely on precise doping profiles and submicron structures to achieve strong light–carrier interaction. Also, the monolithic electro-optic integration process requires aligning metal electrodes to optical waveguides with nanometer precision. This is where the EUV lithography system can leverage its advantages over its DUV predecessor.

Other than creating finer features with better accuracy, the EUV system's more advanced overlay control can improve the alignment between modulator layers and adjacent electronics or waveguides. The EUV lithography method also allows novel modulator architectures to be examined and improved.

3.3. Photodetectors

The superior resolution of the EUV method allows smaller pixels to be created, bringing a more compact design and enhancing the image resolution. EUV lithography also reduces the junction dimension, which decreases photodiode capacitance, lowers the RC time constant, and enables higher output bandwidth.

EUV lithography's precision will create higher fidelity avalanche photodiodes, silicon photomultipliers, and grating couplers, and open the door to novel nanostructures like plasmonic structures or meta-surface, which improves efficiency and light sensitivity.

4. Development and Challenges

4.1. Material Compatibility

One primary challenge lies in the material compatibility of EUV radiation with silicon and other materials commonly used in silicon photonics. The 13.5 nm wavelength EUV light interacts with silicon, silicon dioxide, silicon nitride, germanium, and other thin films and doping profiles in ways that need careful consideration for photonic device performance. The optical properties of EUV-sensitive materials and the impact of EUV exposure on their surfaces and underlying structures relevant to photonics need to be thoroughly understood. Furthermore, the compatibility of EUV photoresists with this diverse range of materials, beyond just silicon, is crucial. Photoresist adhesion, development behavior, and etching characteristics might vary significantly depending on the underlying material, such as silicon versus silicon dioxide.

4.2. EUV Mask Compatibility

Since most materials absorb 13.5 nm wavelength light, EUV lithography relies on reflective masks, which are fundamentally different and more complex to manufacture than the transmissive masks used in DUV lithography. The reflective nature of EUV masks introduces new failure modes and necessitates stringent defect control. Existing EUV mask design tools and workflows are primarily optimized for rectilinear structures in electronic circuits.

For the application of EUV in silicon photonics, the design and fabrication of reflective masks suitable for patterning the specific geometries, including potentially curvilinear features, of photonic devices will be required.

4.3. Photoresist

The photoresists currently used in EUV lithography, often chemically amplified resists (CARs) or metal oxide resists (MORs), have been primarily developed and optimized for silicon-based electronic devices. Applying these resists to silicon photonics manufacturing might require optimization or the development of entirely new formulations tailored for silicon and other photonic materials such as silicon dioxide and silicon nitride. Factors like resist sensitivity at EUV wavelengths, achieving high resolution with minimal line-edge roughness, and ensuring sufficient etch selectivity towards these materials for accurate pattern transfer will be critical. The thin resist layers often employed in EUV lithography could also pose challenges for etching into materials like silicon dioxide or silicon nitride used in photonic waveguides, requiring resists with enhanced etch resistance.

Chemically amplified photoresist is prone to a secondary electron cascade during the EUV exposure. Secondary electron cascade can alter the solubility of photoresist and cause a scattering effect that degrades the patterning quality. Potential alternative non-chemically amplified resists (non-CAR) are being explored for integrating more suitable photoresists for silicon photonics.

4.4. Patterning Requirement

Silicon photonics manufacturing requires the fabrication of curved and complex waveguide geometries, which differ from the primarily rectilinear structures in electronic circuits for which EUV lithography has been primarily developed. The optical proximity correction (OPC) models and mask design rules currently used in EUV lithography might need to be adapted to accurately reproduce these curved shapes in photonic devices. Moreover, the resolution and line-edge roughness (LER) requirements for photonic waveguides, which directly impact optical losses during light propagation, might be different and potentially more stringent than those for electronic circuits. Smooth waveguide sidewalls are essential for minimizing scattering losses in photonic devices, placing demanding requirements on the patterning process.

5. Conclusion

EUV lithography is an advanced photolithography system that can produce chip features below 7 nm, where the previous 193 nm DUV system begins to struggle. A promising candidate for photonic integrated circuits, silicon photonics, is currently fabricated using the DUV lithography process. This article illustrates the basics of the EUV lithography process and systematically analyzes the application of EUV lithography in silicon photonics manufacturing, which presents a pathway towards achieving smaller, more compact, and higher-performance silicon photonic device designs. The article also discussed several technical challenges related to material compatibility, patterning, EUV mask, and photoresist compatibility that need to be addressed before the EUV system can be integrated into silicon photonics manufacturing. The key to next-generation silicon photonics applications and improved performance of future silicon photonic devices may lie in the integration of the EUV-based lithography method. EUV can be expected to bridge between the development of the electronics ecosystem and the emerging photonic integrated circuit ecosystem.

References

[1] Hu Xiaoming, Photolithography technology in electronic fabrication. Advances in Engineering Research, 2015,156.

[2] Yang Dekun, Wang Du, Huang Qiushi, et al. The development of laser-produced plasma EUV light source, Chip, 2022, 1(3).

[3] Shekhar S, Bogaerts W, Chrostowski L. et al. Road mapping the next generation of silicon photonics. Nat Commun, 2024, 15,751.

[4] Mostafa Y, Behnke L, Engels D J, et al. Production of 13.5 nm light with 5% conversion efficiency from 2 μm laser-driven tin microdroplet plasma. Applied Physics Letters, 123(23).

[5] Sato Y, Handa H, Kushida Y, et al. Process bias control with thin Cr film blanks for 90nm-node reticle fabrication. International Society for Optics and Photonics, 2002.

[6] Ma Xu, Wang Zhiqiang, Lin Haijun, et al. Optimization of lithography source illumination arrays using diffraction subspaces. Optics Express. 26. 3738-3755.

[7] Mojarad N, Gobrecht J, Ekinci Y. Beyond EUV lithography: a comparative study of efficient photoresists' performance. Rep, 2014, 5:9235.

[8] Gallagher E, Ragnarsson L K, Rolin C. Sustainable Semiconductor Manufacturing: The Role of Lithography, IEEE Transactions on Semiconductor Manufacturing, 2024(4): 37.

[9] Srivastava K, Le-The H, Lozeman J J A, et al. Prospects of nano-lithographic tools for the fabrication of surface-enhanced Raman spectroscopy (SERS) substrates, Micro and Nano Engineering, Volume 23, 2024, 100267.

[10] Jian Wang, Yun Long, On-chip silicon photonic signaling and processing: a review, Science Bulletin, Volume 63, Issue 19, 2018.

[11] Baets R, Rahim A. Heterogeneous integration in silicon photonics: opportunities and challenges: opinion, Optical Materials Express, 2023, 13(12): 6.

[12] Ye Zhichao, Jia Haiyan, Huang Zhangjun et al. Foundry manufacturing of tight-confinement, dispersion-engineered, ultralow-loss silicon nitride photonic integrated circuits, Photonics Research, 2023, 11(4): 558.

[13] Shahbaz M, Butt MA, Piramidowicz R. Breakthrough in Silicon Photonics Technology in Telecommunications, Biosensing, and Gas Sensing. Micromachines (Basel). 2023 Aug 19;14(8): 1637.