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Improvements on Solution-Based IGZO TFTs Optoelectronic Properties

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Abstract. Indium gallium zinc oxide (IGZO) gained significant attention in the semiconductor and display industries due to its high carrier mobility, excellent flexibility, and superior transparency. These features meet the growing demand for higher resolution and foldable displays. Solution-based IGZO thin-film transistors (TFTs) have demonstrated great potential for reducing production costs and enhancing the optoelectronic performance of display devices. However, several challenges remain, including poor uniformity caused by uneven precursor deposition, high defect state density, which limit the carrier mobility and current controlling capability of the transistor. This paper first introduces the fundamental principles and parameters used to quantify the electric performance of the TFTs. Then ummarizes current optimization strategies such as annealing temperature, metal doping, and substrate material selection, based on the aforementioned performance parameters. Additionally, the effect of embedding an indium zinc oxide (IZO) layer into the Hf-doped IGZO film is discussed, aiming to increase free electron concentration and reduce oxygen defect density. finally, the paper proposes future optimization directions, including the design of multiphase semiconductor structures and the introduction of electromagnetic wave irradiation between pre- and post-annealing steps. These strategies are expected to enable the fabrication of IGZO TFTs with enhanced electrical performance and greater commercial viability.

Keywords: IGZO; solution method; annealing; doping.

1. Introduction

As the advancement of display technology steps towards higher resolution, better flexibility, and transparency, conventional silicon-based materials are increasingly unable to meet these new demands. Indium gallium zinc oxide (IGZO) has emerged as one of the most promising materials for modern display applications.

A notable derivative, IGZO TFT-based organic light emitting diode (OLED) displays offer excellent color reproducing ability and are suitable for flexible display screen manufacturing. However, compared to traditional LCD display technology, OLED displays are relatively expensive. In IGZO TFT fabrication, solution-based methods present a cost-effective alternative to vacuum-based techniques such as magnetron sputtering [1]. The cost reduction primarily arises from simplified precursor deposition and lower annealing temperature requirements. However, a key drawback of solution-based processes is the difficulty in achieving high film uniformity. Poor uniformity leads to increased defect state density, which in turn reduces carrier mobility and the current-switching ratio. Current research focuses on optimizing annealing temperature and doping metals to compensate for the film inhomogeneity caused by solution deposition. These strategies aim to reduce defect density and enhance the concentration of free carriers, thereby improving overall device performance. Nevertheless, fully addressing this issue remains challenging due to the inherent limitations of solution-based deposition methods, such as spin-coating and inkjet printing, which offer limited process control [2].

This paper investigates the effects of annealing temperatures, doping methods, and substrate materials on the electrical performance of solution-processed IGZO TFTs. Four key performance parameters are evaluated to understand how these factors influence device behavior, with particular emphasis on how each strategy affects the density of defect states.

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2. The basic principles and preparation of IGZO TFTs

2.1. Basic structure

TFT is a typical three-electrode active field-effect semiconductor device. It is composed of thin films of semiconductors, metals and insulating materials through deposition [1].

According to the different placing positions of the gate, source and drain, TFT can be divided into four types that are separately bottom-gate top-contact configuration, bottom-gate bottom-contact configuration, top-gate top-contact configuration, and top-gate bottom-contact configuration (Figure 1).

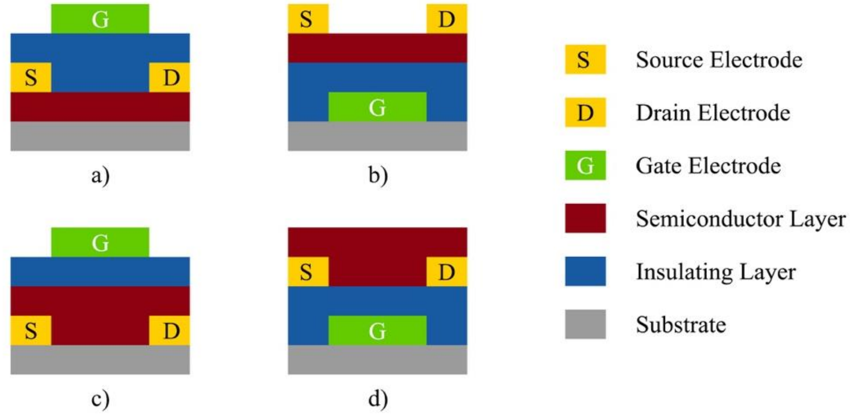

Fig. 1 (a) top-gate top-contact configuration. (b) bottom-gate top-contact configuration. (c)top-gate bottom-contact configuration. (d) bottom-gate bottom-contact configuration.

If the gate electrode lies under the dielectric layer, it is called the bottom-gate while on the contrary, it is called the top-gate. If the source and drain electrode are located above the semiconductor layer, it is called top-contact while on the contrary, it is called the bottom-contact. With a combination with each other, the above four basic structures can be obtained. The bottom-gate structure enables the insulating layer and the gate electrode to be deposited first, thereby preventing the semiconductor layer from crystallizing due to excessively high annealing temperatures or the electrode from oxidizing at high temperatures. In addition, the top-contact structure can increase the contact area between the electrode and the channel to reduce the overall resistance of the device. This is because in the bottom contact structure, only the side of the electrode is the contact surface [1,3].

2.2. Basic working principle

The fundamental function of a transistor is to control the current between the source and drain by adding a gate voltage, thereby acting as a voltage-controlled electronic switch. Specifically, the gate voltage modulates the carrier concentration in the channel region, enabling regulation of the drain current (I_{DS}). There are three basic working status of a TFT, which are separately cutoff region, linear region, and saturation region, classified according to the quantitative relationship of Gate-Source voltage (V_{GS}), Drain-Source voltage (V_{DS}), and threshold voltage (V_{th}).

When the electronic potential difference between gate and source is below the threshold voltage, little carriers are induced in the channel between the drain and the source electrode, making I_{DS} very low. Under this circumstance, the TFT runs for cutting off the current.

When V_{GS} reaches V_{th}, by the gate electrode increasing the induced carrier concentration, carriers accumulate at the interface between the insulating layer and the semiconductor layer, forming an effective conductive channel between the source and the drain electrode.

If $V_{GS} - V_{DS} > V_{th}$, carriers fill the entire channel horizontally and no parts are cut off. According to the experience rule of I_{DS}, the applied gate voltage is directly proportional to I_{DS}, and the TFT is in the linear region.

If $V_{GS} - V_{DS} < V_{th}$, the part close to the drain electrode of the conductive channel is cut off, making IDS irrelevant to the floating of V_{GS}. Therefore, I_{DS}tends to saturate and that's the saturation region of the TFT.

The I_{DS} in the above two cases can be respectively represented by the following experiencing formulas [4].

Linear region:

$$I_{DS} = \frac{WC_i\mu_{lin}}{2L}(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \quad (1)$$

Saturation region:

$$I_{DS} = \frac{WC_i\mu_{sat}}{2L}(V_{GS} - V_{th})^2 \quad (2)$$

Among them, C_i is the capacitance of the insulating layer per unit area, L is the channel length of the semiconductor layer, W is the channel width of the semiconductor layer, V_{th} is the threshold, μ_{lin} is the carrier field-effect mobility in the linear region, and μ_{sat} is the carrier mobility in the saturation region[1,4].

2.3. Solution preparation method of IGZO TFTs

The solution-based preparation process of IGZO TFTs can be generally divided into five steps, precursor synthesis, deposition, pre-annealing, post-annealing, and TFTs fabrication.

IGZO film is the core functional component of IGZO TFTs. The preparation methods can be divided into magnetron sputtering and solution methods. Among them, solution-based production includes spin-coating, inkjet printing, roll-to-roll(R2R), Dip-coating and other methods [2].

Spin-coating involves depositing a precursor solution onto a rapidly rotating substrate, where centrifugal force distributes the liquid uniformly across the surface. This technique can improve the uniformity of the film, whereas it is inclined to causing waste because of splashing and is unable to form large-area films. Inkjet printing deposits the precursor solution in the form of microscopic droplets through a nozzle directly onto the substrate. This method allows precise patterning and spatial control of the film formation. Nevertheless, the equipment required is costly, and the process generally suffers from low throughput. Roll-to-roll (R2R) processing applies the precursor solution to a flexible substrate, followed by repeated rolling and thermal annealing. Its primary advantage is its suitability for continuous, large-scale production, making it ideal for industrial-scale fabrication. Dip-coating involves immersing the substrate into the precursor solution and withdrawing it at a controlled speed. The surface tension will generate an adhesive wetting effect, thereby forming a film on the surface of the substrate. The prominent advantage of this method is that the expansion of the film area barely increases the difficulty of production. Furthermore, with precise control of the withdrawal speed and ambient conditions, the uniformity of the deposited film can be effectively maintained [5].

Precursor synthesis and deposition involve dissolving metal salts into a solvent to ionize the constituent metals, enabling their subsequent deposition onto the substrate to form a uniform thin film. During film formation, the metal cation complexes undergo hydrolysis and condensation reactions, resulting in the formation of metal oxide films, while volatile byproducts are removed from the system. The precursor of IGZO is often prepared by dissolving zinc acetate, indium nitrate and gallium nitrate in 2-methoxyethanol, and ethanolamine is added to the solution as a stabilizer. Subsequently, stir it with a magnetic stirring bar under constant temperature conditions, and then let it stand for aging. Prior to deposition, P-doped silicon substrates are sequentially cleaned with deionized water (DIW), acetone, isopropanol, and again with DIW. This is followed by oxygen plasma treatment to improve surface wettability. Finally, the prepared precursor solution is uniformly dispensed onto the substrate using a pipette, forming the IGZO thin film upon deposition [6].

The subsequent two steps in the fabrication process are pre-annealing and post-annealing, each serving distinct purposes despite both being thermal treatments. Pre-annealing is typically conducted at a lower temperature and for a shorter duration, primarily to remove residual solvents from the precursor film. In contrast, post-annealing is performed at a higher temperature and for a longer time, aiming to complete the hydrolysis and condensation reactions and to eliminate organic impurities, thereby enhancing the optoelectronic properties of the TFTs [7].

The final step is fabrication, which involves integrating the thin films with the electrodes to form a complete TFT structure. The stacking order of the electrodes and active layers during this stage determines the overall architecture of the device (Figure 2).

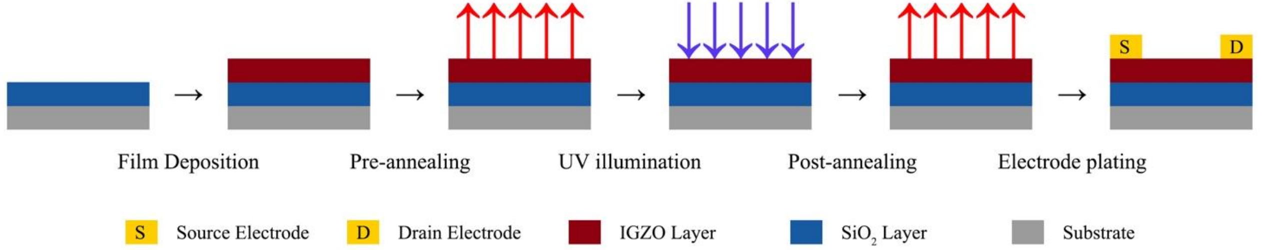

Fig. 2 Solution-based IGZO-TFT producing process

Solution-processed IGZO TFTs offer the advantages of relatively simple fabrication procedures, relaxed processing conditions, and low production costs. However, solution-based deposition also presents challenges, including limited film uniformity and a high density of defect states [3]. Current research efforts focus on improving device performance through strategies such as optimizing annealing temperatures, introducing metal dopants, and refining processing parameters.

3. Characterization Methods and Improvement Approaches for solution -based IGZO TFTs Device Performance

3.1. The main characterization parameters of IGZO TFTs performance

The main variables that indicate the optoelectronic properties of IGZO transistor are carrier mobility (μ), threshold voltage (V_{th}), current switching ratio ($\frac{I_{on}}{I_{off}}$), sub-threshold swing (SS) [4,6].

The carrier mobility is defined as the average drift velocity of carriers under the action of a unit electric field, reflecting the transportation efficiency of the carriers. Therefore, carrier mobility is directly proportional to the velocity of carriers. The carrier mobility of the saturation status can be calculated by applying Eq.(2).

$\sqrt{I_{DS}}$ and V_{GS} have a linear relationship, and its slope K can be calculated after linear simulation. The saturation carrier mobility μ_{sat} has the following relationship with the slope K.

$$\mu_{sat} = \frac{K^2 \cdot 2L}{W \cdot C_i} \tag{3}$$

Here, C_i, W, and L denote the gate capacitance, channel width, and length, respectively.

The threshold voltage corresponds to the gate voltage V_{GS} applied to the conductive channel formed at the interface between the insulating layer and the semiconductor. For a-IGZO devices, when V_{th} is positive, it is an N-channel enhanced TFTs; on the contrary, it is N-channel depleted TFTs. Like the calculation of the saturation region carrier mobility, it is found that V_{th} is exactly the intercept of the linear function of $\sqrt{I_{DS}}$ and V_{GS} on the X-axis. This linear relationship can be calculated through linear simulation.

The current when a transistor is completely conducting under the action of the gate voltage is called the open-state current(I_{on}) while the leakage current of a transistor when the gate voltage is zero or

insufficient to conduct is called the off-state current(I_{off}). The current switching ratio is defined as the division of the on-state current and the off-state current($\frac{I_{on}}{I_{off}}$). It reflects the current control capability of a transistor in both on and off states.

The subthreshold swing is defined as the derivative of the gate voltage to the drain-source current's logarithm, and thus also reflects the changing sensitivity of the gate voltage along with the drain-source current, and this variation relationship is negatively correlated. The main factors that influence sub-threshold swing are the defect density of semiconductor layers and the defect density at the interface between semiconductor layers and insulating layers.

$$SS = \frac{d(V_{GS})}{d(\log I_{DS})} \tag{4}$$

3.2. Annealing temperature and auxiliary conditions

Annealing is an essential step in the fabrication of thin-film transistors, particularly for improving the quality and performance of solution-processed devices. The thin film depositon may lead to non-uniform or poorly distributed films, resulting in defects such as oxygen vacancies and residual impurities. Annealing treatment can promote the rearrangement of atoms through thermal energy to fill defects and reduce the negative impact of these defects on the performance of the device. Furthermore, annealing promotes the crystallization of semiconductor materials, which is beneficial for enhancing carrier transport.In 2022, Chong et al. [3] investigated the transfer characteristics of IGZO-TFTs fabricated under different post-annealing temperatures. During the process of increasing the post-annealing temperature from 270 °C to 400 °C, the saturation carrier mobility, threshold voltage, sub-threshold swing, and the current switching ratio all fluctuate. In the experiment, the post-annealing temperature of 360 °C shows the best optoelectronic properties especially compared to lower temperature. This is because under low temperature annealing conditions, the condensation and densification reaction process of IGZO thin films is relatively low, the proportion of stable metallic oxygen bond structures is relatively small, and the residual hydroxyl content is relatively high.

Additionally, transfer curve analysis revealed that ultraviolet (UV)-assisted annealing can further enhance device performance. UV exposure during annealing reduces the density of defect states, leading to improved stability of I_{DS} in the saturation regime and enhanced gate voltage modulation capabilities [1].In 2023, Li et al. [8] conducted a related study on IGZO active layers deposited on SiO_2 substrates using a solution process. The results showed that annealing at 550 °C yielded the best electrical performance, with a current on/off ratio reaching 10^5 and stable operational characteristics. As the annealing temperature approached this optimal point, the densification of the film increased, metal-oxygen bond formation was enhanced, and defect state density decreased. These changes reduced electron trapping and scattering, thereby improving carrier mobility and overall device performance.

In 2024, Moon et al. [9] proposed an alternative annealing approach using intense pulsed light (IPL). In their method, the IGZO precursor layer was pre-treated with near-infrared (NIR) and deep ultraviolet (DUV) light. The combined irradiation promoted rapid drying and initiated Ga–O bonding, suppressing excess carrier generation during subsequent IPL processing. Compared to traditional thermal annealing, which requires exposing the device to air for a long time, IPL annealing can reduce the contact between the thin film and the outside environment so as to minimize impurity intrusion, and enhance device performance. The experiment also thoroughly considered the impact of IPL energy levels on the electrical performance of TFTs. When the IPL energy is low, the IGZO layer has low crystallinity, resulting in low carrier mobility. Conversely, when the IPL energy is too high, it forms a highly conductive film with high carrier mobility, leading to an increase in off-current and a decrease in the current switching ratio. Therefore, the IPL energy level also needs to be strictly controlled to achieve optimal device performance.

In summary, solution-processed IGZO TFTs offer a significant advantage in terms of compatibility with low-temperature annealing[3]. However, their output characteristics can still be improved. Strategies such as UV or IPL-assisted annealing have demonstrated promise in enhancing film quality and device performance by reducing defect density and promoting optimal electronic structure formation.

3.3. Metal doping

IGZO-TFTs fabricated via solution-based methods benefit from simplified processing conditions and lower production costs. However, such devices typically exhibit a higher density of defect states, which can significantly impair their electrical performance. Beyond the annealing treatments previously discussed, doping emerges as another effective strategy to mitigate these defects. By incorporating metal dopants, vacant lattice sites can be filled and additional free electrons can be introduced, thereby modifying the film's electronic properties. Lithium has become an ideal choice for doping metals due to its small atomic volume low standard electrode potential. Small volume enables it to fill in minute gaps. Low standard electrode potential makes it to lose electrons easier to combine with oxygen.

In 2020, Jang et al. [10] measured the crystallinity of the Li-IGZO films on SiO_2/Si wafer substrates using X-ray diffraction. XPS spectra result shows that the doping of Li metal can significantly reduce the oxygen vacancy rate in IGZO films. Among all the matched groups, the oxygen vacancy rate of the IGZO film with 5% Li doped decreased most significantly from 19% to 7% compared to that of undoped IGZO film. In 2024, Kim et al. [11] explored the effects of hafnium (Hf) doping. To eliminate the influence of the gate dielectric layer, the experimenters deposited a thin Hf film on the channel layer. Additionally, a thin IZO layer was deposited on top of the Hf film. After annealing, IZO layer combines with the surrounding oxygen, thus reducing the oxygen vacancy density. The experiment found that Hf ions hardly enter the upper IZO layer. This can be attributed to the ionic radius of Hf being larger than that of In^{3+} and Zn^{2+} ions. Therefore, higher binding energy is required to enter the IZO layer. However, Hf ions have a high binding energy with oxygen vacancies. Under the combined effect of both, Hf ions can efficiently and selectively bond with oxygen ions, reducing the defect density and enhancing device performance. The study also observed that high-temperature annealing led to an increase in oxygen vacancies within the IZO layer, as oxygen ions were extracted by Hf, generating additional free electrons and further improving the electrical conductivity of the TFT.

In summary, appropriate metal doping is an effective method to improve the optoelectronic properties of IGZO films by passivating defect states and modulating carrier concentration. Furthermore, surface coating with electron-donating materials may offer additional performance enhancement. However, the optimal choice of materials for such coatings remains an area for further exploration.

4. Conclusion

This paper reviews recent research on the solution-based preparation of IGZO TFTs, focusing primarily on the variation in optoelectronic performance parameters with different annealing temperatures and the effects of Lithium and Hafnium ion doping in reducing defect state density. It is found that the primary limitation in device performance stems from the non-uniformity of thin films produced by solution deposition. Some research experimental results show that device performance can be significantly improved by precisely controlling the annealing temperature and selecting Li with a small atomic radius as the doping metal. Moreover, the IZO layer deposited more innovatively in the channel layer can enhance the electrical conductivity and electron mobility from the perspective of free electron density.

Solution processing has become an essential method for fabricating IGZO TFTs due to its low thermal budget and suitability for large-area manufacturing. However, it still suffers from several limitations, indicating substantial room for further research. For example, future work could explore the use of

multi-layer metal oxide films with varied compositions to concentrate free electrons in the IGZO layer, or the application of external conditions during annealing to improve film dehydration, cooling efficiency, and overall uniformity. Employing dopants with different ionic radii may also contribute to a lower density of defect states. Persisting in the in-depth exploration and research of semiconductor science that integrates disciplines such as chemical physics and electrical engineering is the key to pushing IGZO TFT to the forefront of contemporary transistor technology and is also the cornerstone that brings its commercial value.

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