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Research on CMOS Devices Based on Wide Bandgap Semiconductor Materials

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Abstract. Considerable financial resources have been allocated towards the design and development of wide and ultra-wide bandgap semiconductor circuits due to their use in power and radio frequency electronics. This is due to the fact that these circuits possess the capability to accomplish these tasks. Due to their minimal loss rates and capacity to rapidly switch high currents and voltages, these devices exhibit great versatility. The presence of parasitic effects in silicon-based CMOS circuits, which are necessary for the integration of intricate control logic, often hinder the performance of end systems that use these devices. This is a difficulty since these circuits are crucial for the execution of intricate control logic. A viable technique that has recently evolved involves directly incorporating CMOS circuitry into a wide bandgap substrate, which is suitable for a range of mature materials. This approach has developed a functional technology. The objective of this study is to examine the present condition of CMOS technology in wide bandgap materials such as diamond, SiC, and GaN, with the aim of analysing its current situation. The findings of this study article provide useful insights that might be used in the advancement of energy-efficient electronic gadgets with enhanced performance capabilities.

Keywords: CMOS; wide band-gap semiconductor; SiC, GaN.

1. Introduction

In a future characterized by widespread interconnection and energy efficiency, the importance of power and RF electronics is increasing. To meet the stringent performance requirements in these areas, higher conductivity, faster operating transistors in smaller packages at higher voltages are required. Using the complementary properties of NMOS and PMOS transistors, CMOS technology has played an important role in this breakthrough due to its high efficiency and low power consumption. CMOS circuits consist of two complementary NMOS and PMOS transistors for each logical unit. Since the current only passes through the circuit when it is switched on and off, these circuits have very low static power consumption, which emphasizes their great potential.

MOSFETs' physical dimensions have progressively shrunk from 180 nm to 90 nm, 45 nm, and 22 nm, and they have now reached the age of less than 10 nm as a result of rising demands for improved efficiency and lower costs. However, leakage currents, short-channel effects (SCEs), and parasitic capacitors and resistors are among the difficulties brought on by this miniaturisation. The progress of CMOS technology has been severely impeded by these issues. To solve these problems, scientists have created a number of cutting-edge methods, including high-k metal gate (HKMG) technology, silicon on insulator (SOI) architectures, and FINFET designs. While these advancements have lessened some of the issues related to overheating and leakage currents, they have proven ineffectual at lower technological nodes. Standard silicon-based CMOS technology is challenged by the growing need for high voltage and high power consumption applications.

The emphasis of current research is on semiconductor materials with broad gaps. These materials have excellent breakdown voltage, electron mobility, and thermal conductivity, which make them suitable for a variety of high-power, high-frequency applications. Semiconductors often have band gaps larger than 2.2 eV. They can function correctly at greater temperatures and voltages because to this characteristic, which also reduces leakage current. In order to find out how wide band gap semiconductor materials may solve the drawbacks of conventional silicon-based technologies and

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open the door for next-generation electronic devices, this research examines the special uses and benefits of these materials in CMOS devices.

2. Foundation and Development of CMOS

2.1. Development of CMOS

The exploration began with vacuum tubes and bipolar junction transistors, but it was the advent of MOSFETs that truly triggered the explosive growth of information technology, as shown in Figure 1. The inherent characteristics of NMOS and PMOS transistors are crucial for the functioning of CMOS. A CMOS logic gate consists of a combination of NMOS and PMOS transistors working together to form the logic unit. When the input signal is high, the NMOS transistor is active, and the PMOS transistor is inactive, resulting in a low-level output. When the input signal is low, the PMOS transistor turns on, the NMOS transistor turns off, and the output is high.Since current only exists during the switching state, CMOS circuits exhibit almost no power consumption in static conditions. This feature makes them highly promising for high-speed, high-density, and low-power VLSI applications. Consequently, the continuous reduction in the physical size of MOSFETs has become a widely recognized development direction. From 180nm, 90nm, 45nm to 22nm, each reduction in size has led to increased transistor density and reduced power consumption. After 2020, the size of CMOS devices has even entered the sub-10nm era.

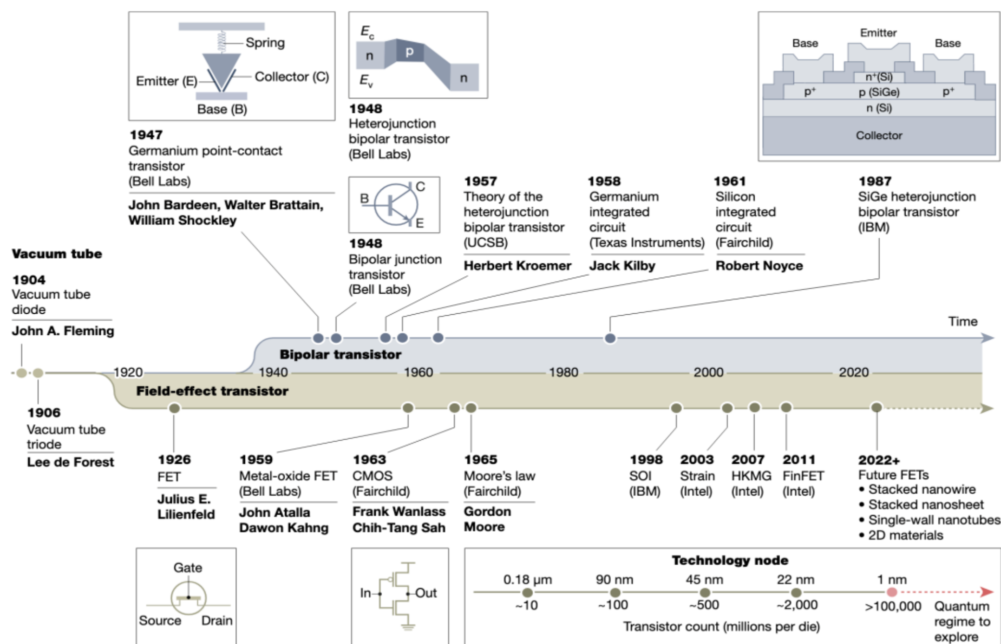

Figure 1. The history of transistor technology [1].

2.2. Limitations of CMOS

Early CMOS technology research primarily focused on fabricating source, drain, and channel doping distributions and reducing the thickness of the physical gate oxide layer. However, as the physical gate length continues to shrink, certain issues, particularly short-channel effects (SCEs), have increasingly limited the advancement of CMOS technology. As the gate size decreases, the channel potential is influenced by the drain and source. This results in a reduction in gate efficiency, a primary outcome of SCEs. As the drain bias increases, the potential barrier in the channel decreases, leading to a reduction in the threshold voltage. This directly results in non-ideal current saturation in the output characteristics. The smaller the transistor gate length, the more severe the short-channel effects, and the poorer the device's switching characteristics. Additionally, parasitic capacitance and resistance increase with size scaling. Moreover, size reduction also significantly increases leakage current.

Leakage current primarily arises from the following mechanisms: direct tunneling , Fowler-Nordheim tunneling, and hot carrier injection-induced gate leakage; sub-threshold leakage; direct source-drain tunneling leakage; reverse-biased diode leakage; and junction leakage caused by gate-induced drain leakage [1]. These leakage current mechanisms collectively contribute to an increase in the power consumption of the devices.

2.3. Optimization Solutions for CMOS

The development of CMOS technology faces not only issues such as short-channel effects, parasitic capacitance, parasitic resistance, and leakage current. The demands for high integration and high response speed also lead to increased power density in chips, making thermal management and power consumption control more complex. To overcome the bottlenecks of traditional CMOS technology, researchers have made various attempts. In modern scaling strategies, new materials and device architectures have been introduced.

Firstly, the use of high-k dielectric materials such as Hafnium oxide increases gate capacitance, thereby reducing leakage current and significantly improving device switching speed and reliability [2]. Additionally, researchers are exploring materials with higher mobility to replace the traditional Si channel. For instance, using InAs in vGAAFET as the nMOS channel material and Ge or SiGe as the pMOS channel material has become an ideal high-mobility option since the advent of the 10nm technology node. The electron mobility of InGaAs is 4000 $cm^2/V \cdot s$, and the hole mobility of Ge is 1900 $cm^2/V \cdot s$, compared to the conventional Si channel's 1400 $cm^2/V \cdot s$ and 450 $cm^2/V \cdot s$, respectively [3].

In addition to material improvements, significant research has been conducted on 3D structures and strain engineering in modern transistors, unlike past planar 2D transistors. These efforts aim to further reduce the size of gate and source/drain regions, achieving higher integration and lower interconnect delay. In ongoing research, device shapes have evolved from simple fin structures to fully depleted insulators or nanowires, such as Fin-on-Insulator (FOI), FinFETs, tapered FinFETs, and nanowire FETs. Research findings indicate that these innovative 3D transistor architectures can indeed better control short-channel effects and enhance device performance.

Fully Depleted Silicon on Insulator (FDSOI) forms a fully depleted structure by growing a thin silicon layer on an insulator, thereby reducing short-channel effects and leakage currents. FDSOI technology is a common method for controlling SCEs during transistor size reduction. Constructing FinFETs on insulators, known as FOI, combines the advantages of SOI and FinFET technologies, demonstrating higher device performance. This presents a highly promising research direction for future transistor design [3].

Since the introduction of the FinFET structure into traditional MOSFETs, the multi-gate design has significantly enhanced control over the channel, effectively reducing leakage current and improving the electrostatic control of the device. Researchers have also incorporated high-mobility materials such as InGaAs and SiGe into FinFETs, further boosting their performance. The high mobility characteristics of these materials result in substantial improvements in current density and switching speed for FinFETs.

Moreover, FinFETs show considerable potential in power consumption and thermal management. Due to their unique three-dimensional structure, FinFETs exhibit higher thermal stability and lower power consumption. This makes them highly suitable for applications requiring high performance and low power, such as mobile devices and the Internet of Things (IoT) [2].

Gate-All-Around (GAA) Field-Effect Transistors (FETs) are highly regarded as promising candidates for technology nodes of 3nm and below. This is especially true for vertical Gate-All-Around Field-Effect Transistors (vGAAFETs), which offer a high degree of integration versatility. Multiple studies have shown that a silicon substrate can be used to form a complex structure consisting of p-Si, i-SiGe, and p-Si layers. This structure is often used in the design of vGAAFETs.

3. Research on Wide Bandgap CMOS Devices

3.1. Wide bandgap semiconductor

However, despite these technological advancements in mitigating SCEs and leakage currents, limitations still exist when applying them to smaller technology nodes. conventional CMOS technology struggles to meet the growing demand, particularly in applications requiring high power and frequency. To address these issues, researchers have turned their attention to wide bandgap semiconductor materials. These materials have exceptional thermal conductivity, high electron mobility, and elevated breakdown voltage, providing significant advantages for various specialized applications.

Materials with a bandgap exceeding 2.2 electron volts (eV), as shown in Figure 2, are commonly referred to as wide bandgap semiconductor materials. Materials with larger bandgaps have a remarkable ability to maintain their electrical properties even when exposed to external factors like electric fields or heat. This is because larger bandgaps enable a higher maximum electric field blocking capacity (Emax) [4]. Compared to traditional silicon-based materials, these materials have the capability to function at elevated voltages and temperatures while minimising leakage currents and maximising efficiency.

To overcome the limitations of conventional CMOS technology and explore new opportunities for developing efficient and powerful electronic devices, examining the integration of wide bandgap semiconductor materials is desirable.The following sections will explore the specific applications and advantages of wide bandgap semiconductor materials in CMOS devices in detail.

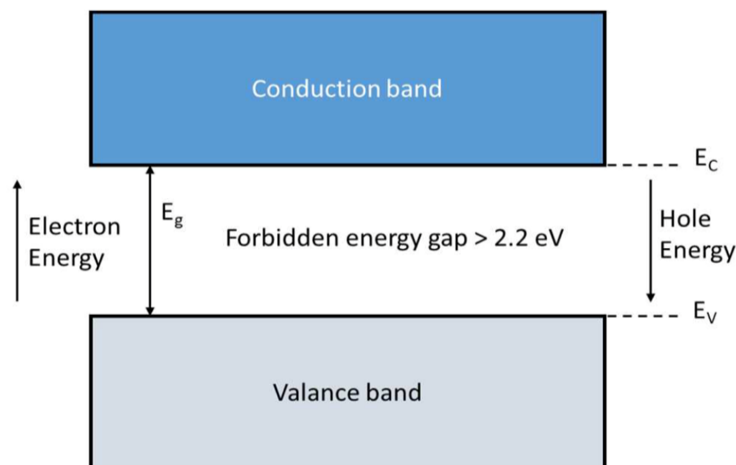

Figure 2. Energy band diagram for WBG semiconductor [5].

3.2. Silicon Carbide

SiC and GaN, the most commercially successful wide bandgap semiconductor materials, have garnered significant interest from researchers due to their much higher performance compared to Si, as shown in Figure 3. First, the introduction of SiC semiconductor material is discussed. The commercial maturity of silicon carbide light-emitting diodes marked the emergence of wide bandgap semiconductor materials as a focus of research. Compared to traditional Si-based devices, SiC vertical power devices will hold an advantage for a long time, especially in applications requiring high voltage blocking capability. However, SiC CMOS devices still need to overcome several obstacles. The primary concerns are the limited mobility of the inversion channel and the high density of interface traps at the SiC-oxide interface. Among the three primary polytypes of SiC (3C, 4H, 6H), 3C-SiC has the highest SiO_2 interface quality. However, its practical applications are limited due to its narrower energy bandgap and subpar bulk epitaxy quality. While 6H-SiC exhibits higher MOS inversion

channel mobility, its higher bandgap still fails to meet commercial demands. In comparison, 4H-SiC is widely used in power devices due to its extraordinary physical properties, such as superior thermal conductivity, increased breakdown electric field strength, and enhanced electron mobility [6].

The typical mobility range for the nMOS inversion channel is 25-35 cm²/Vs. Although procedures incorporating the diffusion of additional elements into the oxide have achieved high mobilities of 100 to 200 cm²/Vs, these devices still lack stability at high temperatures. The superior thermal conductivity of SiC can somewhat mitigate these issues. Currently, the lateral SiC nMOS mobility is about 500 cm²/Vs, while the typical mobility of GaN/AlGaN 2DEG is 1500-2000 cm²/Vs, indicating a significant gap between the two [7].

By the end of the 20th century, advancements in design and development led to significant reductions in the specific on-resistance of SiC power MOSFETs.Subsequent research has further developed SiC power MOSFETs in high voltage and high frequency applications. The commercially available SiC power MOSFETs currently have a rated voltage of up to 3.3 kV [8]. Since the ideal SiC power MOSFET chip (10 kV, Ron,sp = 127 mΩ·cm²) was reported in 2011, SiC power MOSFETs with Ron,sp of 169 mΩ·cm² at 13 kV and Ron,sp of 210 mΩ·cm² at 13 kV have gradually entered the public eye [9]. However, as research progresses, several challenges continue to impede technological advancement. For instance, SiC devices need to use ion implantation processes to define channel lengths, as traditional double diffusion processes are not suitable for SiC devices. Moreover, gate oxide breakdown may be attributed to the intense electric field generated in the drift zone of SiC devices in high voltage blocking states. Furthermore, SiC power devices have a relatively limited capacity to endure short circuits. Comparing the SC withstand time of a standard Si IGBT, which exceeds 10 µs, to that of a 1.2 kV conventional commercial SiC power MOSFET under 800V drain bias and 20V gate bias, which is just 3.6 µs, reveals a significant disparity [9].

Despite these challenges, SiC's exceptional thermal conductivity, low inherent carrier concentration, and high breakdown strength make it valuable in demanding environments and operational control points. SiC has emerged as a pioneer in wide bandgap systems, demonstrating its ability to implement complex CMOS circuits. This accomplishment has undoubtedly inspired other emerging wide bandgap CMOS competitors.

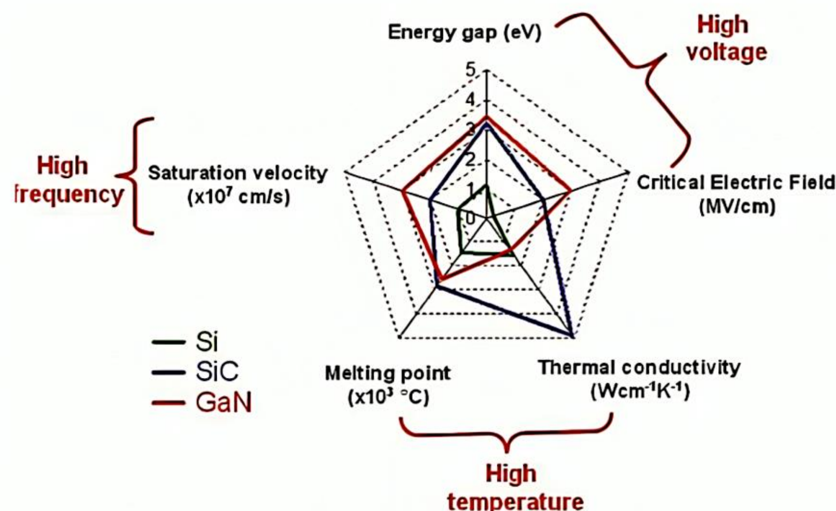

Figure 3. A comparison of wide bandgap materials to Si [10].

3.3. Gallium Nitride

Unlike SiC CMOS, GaN CMOS has not yet achieved mass production. GaN was first successfully commercialized in the field of semiconductor lighting as a key material for blue LEDs, which subsequently spurred a wave of research into GaN materials. The electrical properties of GaN are superior to those of SiC. GaN has a wider bandgap, higher electron mobility, stronger breakdown

electric field strength, and faster carrier saturation velocity. These features give GaN a significant advantage in minimizing on-resistance and switching time, meeting the requirements for applications that prioritize efficiency and power density.Inspired by the AlGaAs/GaAs heterojunction, the AlGaN/GaN heterojunction with high carrier concentration and high mobility has been successfully applied to the fabrication of High Electron Mobility Transistors (HEMTs). This structure, with its naturally formed two-dimensional electron gas (2DEG) channel due to GaN's polarization characteristics, exhibits excellent conduction and switching properties.

For nMOS, this heterostructure differs from traditional MOSFETs in two ways. First, the typical gate stack directly employs metal on the epitaxial surface with aluminum nitride as the barrier layer. Additionally, baseline devices exhibit depletion-mode characteristics due to the abundance of positive polarization charges.However, various techniques have demonstrated the feasibility of enhancement-mode operation, including gate recess, fluorine implantation, fin/trigate, and the most popular p-(Al)GaN gate [7]. Enhancement-mode devices for power applications can provide output currents in the range of hundreds of mA/mm and breakdown voltages of several hundred volts. It is evident that the performance of GaN nMOS devices is significantly superior to that of the aforementioned SiC nMOS devices. In contrast, pMOS still has considerable room for development.

The development of GaN pMOS devices faces many challenges, including deep energy acceptors, difficulty in establishing ohmic connections due to the deep valence band, insufficient mobility, and the scarcity of high-quality holes. Researchers have used material polarization to induce hole gases, partially circumventing the challenges associated with doping. Various heterojunctions, such as GaN/AlN, GaN/AlGaN, InGaN/GaN, and AlGaN/GaN, have been extensively researched for their ability to generate a two-dimensional hole gas (2DHG). Another main challenge for such structures is establishing ohmic contacts. The best results to date involve heavily doping an InGaN layer on a high-density (4-5×10^13/cm²) hole gas of GaN/AlN, achieving contacts in the milliohm range [11].The final limitation is mobility. The low mobility issue arises from the band-edge availability of heavy hole (HH) bands, which have a high effective mass and a high density of states (DOS) that both heavy and light holes (LHs) can scatter to. However, improvement is possible through strain engineering techniques. For example, biaxial tension can enhance split bands, while in-plane uniaxial strain can break HH/LH degeneracy. These methods are estimated to ideally increase mobility to 60-120 cm²/Vs [7].

3.4. Diamond

To further enhance the potential of GaN and SiC in high-temperature and high-power operations, researchers have begun developing wider bandgap semiconductor materials, including Ga_2O_3, diamond, AlN, and BN [12]. However, achieving conductivity and successfully controlling the electrical properties of these ultra-wide bandgap semiconductor materials pose significant challenges. Currently, there have been some breakthroughs in the semiconductor device applications of AlN and diamond, with diamond research even predating that of GaN. As early as the mid-20th century, M. D. Bell et al. published research on natural p-type diamond power diodes [13]. Diamond material, with its excellent thermal conductivity and electrical properties (as shown in Figure 4), demonstrates immense potential for applications in high-temperature, high-frequency, and high-power electronic devices.

Despite this, the development of diamond transistors still faces many technical challenges. The manufacturing process of diamond transistors is technically complex and costly. Additionally, due to diamond's extremely stable crystal structure, doping is particularly difficult, especially n-type doping, which is far more challenging than p-type doping. Impurities such as phosphorus (P) and nitrogen (N) have deep donor levels in diamond, often leading to local lattice distortions and high activation, which in turn affects the overall conductivity of the device. Recently, Liao et al. fabricated n-type diamond MOSFETs based on electron-grade phosphorus-doped n-type diamond epitaxial layers, which exhibited excellent electron mobility in tests, laying the foundation for subsequent research [14]. However, given the scarcity of n-channel diamond devices and the limitations of diamond substrates,

researchers have been exploring the combination of diamond, a high thermal conductivity insulator, with GaN transistors to further advance diamond CMOS integration.

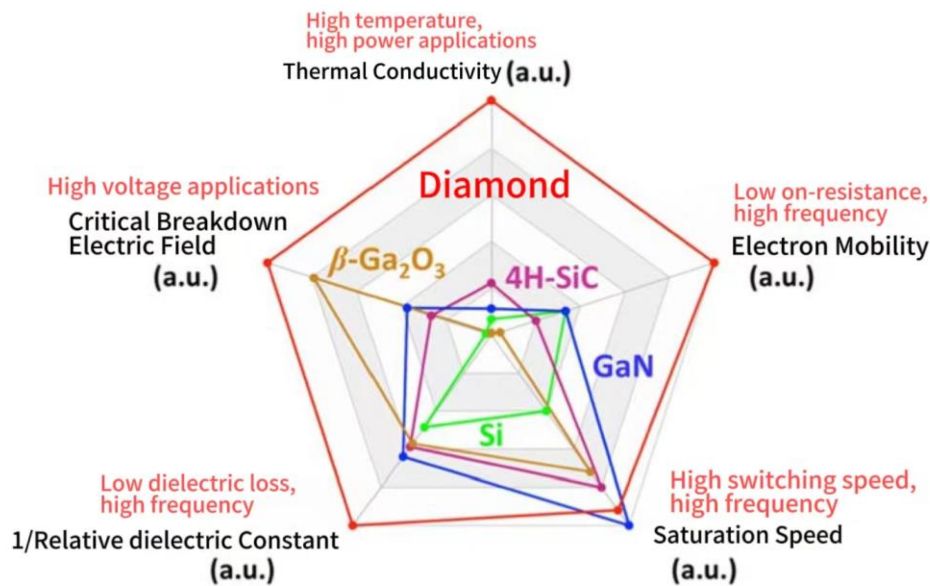

Figure 4. Characteristics advantages of diamond compared to other common semiconductor materials [15].

4. Conclusion

This study investigates the use of wide-band gap semiconductor materials in CMOS technology. Finding the benefits and drawbacks of employing conventional wide-band gap materials like SiC and GaN was the study's primary objective. Additionally, it looks at the potential use of UWB semiconductor materials in CMOS technology. SiC is frequently employed in power devices because to its unique features, which include increased thermal conductivity, enhanced electron mobility, and high electric field strength at breakdown. Nevertheless, there are still several challenges to overcome, including the restricted mobility of the inversion channel and the substantial occurrence of interface trap density. Second, GaN, with its excellent electron mobility and high power density, has become the ideal material for HEMTs. Although the development of pMOS devices faces challenges, its future prospects are promising. Lastly, diamond, known for its exceptional thermal conductivity and electrical properties, holds significant promise for use in electronic devices operating at high frequencies and power levels.However, its manufacturing process is complex and costly, particularly for n-type doping.

Overall, wide bandgap semiconductor materials offer substantial advantages in enhancing CMOS device performance. However, to fully harness their potential, numerous technological challenges must be overcome first. Research progress is expected to significantly influence the advancement of future CMOS technology through the integration of wide bandgap semiconductor materials. This will enable the exploration of new research domains and potential solutions for developing cutting-edge electronic devices with minimal energy consumption.

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