

Design and Optimization of High-Voltage MOSFETs

Chuanjie Wang *

College of Engineering, Beijing University of Technology, Beijing, China

* Corresponding Author Email: ChuanjieWang@emails.bjut.edu.cn

Abstract. Silicon carbide (SiC) power devices have gained significant attention due to their broad applications in high voltage, high frequency, and high temperature environments. Traditional silicon (Si) power devices, although well-established, face performance limitations that SiC devices can overcome. High-voltage 4H-SiC MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) devices are essential for the advancement of power electronics, and this work focuses on their design and optimization. First, a brief summary of the state of research on high-voltage 4H-SiC MOSFET devices is given, highlighting advancements and ongoing efforts in this field. Finally, the study delves into the design optimization of 4H-SiC MOSFET devices at high voltages, describing the vital design parameters and innovative techniques such as multi-zone modulation field limiting ring technology. The findings from this research provide valuable insights and practical guidance to improve SiC MOSFET devices' reliability and effectiveness, building upon the discussed design parameters and innovative techniques. This study significantly contributes to the manufacturing and utilization of electrical devices, promoting more efficient and reliable power conversion solutions in various high-demand sectors.

Keywords: High-Voltage 4H-SiC MOSFETs; Silicon Carbide (SiC) Power Devices.

1. Introduction

As society develops, the continuous consumption of fossil fuels and increasing environmental issues highlight the need for efficient electrical energy conversion to achieve energy-saving and emission-reduction goals. Power devices, especially those based on silicon (Si), have matured over decades but are limited by Si's intrinsic properties [1]. 3rd-generation semiconductors, such as silicon carbide (SiC), are essential for power electronics because of their exceptional characteristics: a high bandgap (3.26 eV), high breakdown electric field (2.5×10^6 V/cm for 4H-SiC), and high thermal conductivity (4.9 W/(cm·°C)). These characteristics make SiC ideal high voltage, high frequency, and high temperature applications, enhancing device reliability and efficiency [2].

The inception of SiC power devices commenced during the early 1950s but progressed slowly until advances in 4H-SiC single-crystal growth technology enabled high-quality, large-diameter SiC wafers. Today, 4H-SiC MOSFETs are used in power electronics, aerospace, and automotive electronics, showing significant market potential. High-voltage 4H-SiC MOSFETs are a research hotspot due to their benefits in applications that involve high temperatures, high frequencies, and high levels of power. Internationally, companies like Cree, Infineon, and ROHM have advanced 4H-SiC MOSFET research. For instance, S.H. Ryu et al. published a study on a 10 kilovolt 4H-SiC MOSFET, which demonstrated a specific on-resistance of 123 milliohms per square centimeter in 2004, and subsequent optimizations reduced this further [3].

In China, research has focused on 600V to 1700V SiC MOSFETs, with notable developments from the University of Electronic Science and Technology of China and the 13th Research Institute of China Electronics Technology Group Corporation [4]. However, ultra-high-voltage research (above 10kV) is still emerging. Optimizing high-voltage SiC MOSFET design requires simulation software like Silvaco to fine-tune parameters such as cell structure, P-base doping, gate oxide thickness, and JFET region length. Multi-zone modulation field limiting ring technology is proposed to optimize terminal design, enhancing breakdown voltage [5].

SiC MOSFETs offer significant value beyond traditional power electronics, reducing converter switching losses, increasing power density, and decreasing system size and complexity [6]. They are suitable for applications in power supplies, rail transportation, motor control, electric vehicles, and aerospace systems. This study offers a theoretical framework and practical instructions for the design and optimization of high-voltage, high-power SiC MOSFET devices, contributing to the technological advancement and broader application of power electronic devices.

2. Current Status of Sic MOSFET Device

2.1. Advantages of SiC Power MOSFETs Compared to Other Switching Devices

SiC power MOSFETs possess inherent advantages over other types of switching devices in medium to low power applications. Due to the simplicity of power circuits and gate drive circuits, silicon carbide MOSFETs are more readily accepted in the industry compared to silicon carbide junction field-effect transistors (JFETs) and bipolar junction transistors (BJTs).

Comparison with SiC JFETs: Although both are unipolar devices, SiC power MOSFETs feature lower gate current and higher input impedance. Compared to normally-on JFET devices, SiC power MOSFETs have simpler drive circuits, and compared to normally-off JFET devices, SiC power MOSFETs have a higher gate drive voltage tolerance.

Comparison with SiC BJTs: BJTs are current-controlled devices, whereas MOSFETs are controlled by voltage and do not necessitate high peak currents for fast turn-on and correct conduction operation. As majority carrier devices, MOSFETs avoid the minority carrier storage issue present in power bipolar transistors, resulting in higher operating frequencies.

Comparison with SiC IGBTs: SiC power MOSFETs, as unipolar devices, exhibit higher operating frequencies in comparison to silicon carbide insulated-gate bipolar transistors (IGBTs). However, because of the restricted mobility of unipolar power devices, their voltage application range is generally considered to be below 10 kV. IGBTs, due to the presence of minority carrier storage time, have lower operating frequencies.

2.2. Advancements and Market Integration of SiC Power MOSFETs

High-frequency electronic power systems require MOSFETs and SiC IGBTs. Their role is critical control for high-power applications. Silicon-based MOSFETs can withstand 1200 V. Si MOSFETs with ratings above 300 V have a much higher on-resistance, requiring larger chip areas to accommodate the rated current. The resistance of silicon (Si) MOSFETs increases by 125% when the junction temperature rises from 25°C to 135°C, while SiC MOSFETs only increase by 20%. Si-based MOSFETs can handle 200 V and 100 A. MOSFETs that can withstand 1200 V usually have a rated current of less than 10 A [7]. Si IGBT devices can handle higher rated current, so they are used for voltages over 600 V. Due to minority carrier storage, IGBT reverse recovery times are long. This limits their switching speed to 20 kHz. However, SiC MOSFETs reduce current reversal time, enabling switching frequencies of up to 100 kHz and higher power density. SiC MOSFETs can operate at 300°C, almost twice the temperature range of Si IGBTs. SiC MOSFETs leak 100 times less than Si IGBTs at high voltages. SiC MOSFETs have 1.6 V lower forward voltage drop than Si IGBTs at 250 A drain current. Therefore, SiC MOSFETs have lower conduction losses. Silicon carbide (SiC) MOSFETs can replace Si IGBT devices in power switches with blocking voltages from 300 to 4500 V. This substitution can significantly improve system switching speed and reduce switching losses [8].

The first commercially available planar gate 1200 V SiC MOSFET (CMF20120D) was introduced by Cree in 2011. Rohm engineered 600 V trench-type SiC MOSFETs the following year. In subsequent years, Cree released planar gate SiC MOSFETs with 900 V, 1000 V, and 1700 V voltage ratings. Ion implantation creates the simple planar gate structure, which is the main device structure for SiC power MOSFETs. Ruhm's SiC MOSFETs use trench gate designs to reduce cell size, increase

cell density, eliminate the JFET region, and reduce conduction losses. Infineon introduced its first asymmetric trench-type SiC MOSFET in 2017. A large p-type region surrounds the trench bottom, improving body diode conductivity, reducing switching losses, and protecting the gate oxide layer near the trench corner from high electric fields by preventing premature gate breakdown. Cree, Rohm, and Infineon recently introduced SiC MOSFET devices with different voltage and current ratings, expanding practical applications. Domestic SiC power MOSFET research began late. The 55th Research Institute of China Electronics Technology Group Corporation (CETC), the 13th Research Institute, Xi'an University of Electronic Science and Technology, and the Chinese Academy of Sciences Institute of Microelectronics developed SiC MOSFET samples with 900 V, 1200 V, and 1700 V voltage ratings. 3. Working Principles and Structures of 4H-SiC MOSFETs [9].

3. MOSFET Devices

3.1. Working Principle of 4H-SiC MOSFET Devices

The operation of 4H-SiC MOSFETs devices is based on forming a conductive channel in the semiconductor material. This occurs under the influence of gate voltage. When a voltage V_{GS} greater than the threshold voltage V_{th} is applied to the gate, electrons in the n-type SiC are drawn towards the gate, creating an inversion layer. The inversion layer serves as the conductive pathway, enabling the flow of current between the source and drain.

Being a device that is controlled by voltage, the 1200V 4H-SiC MOSFET controls its operating state by adjusting the gate voltage V_{GS} . When the gate voltage V_{GS} is 0V, the device is in a state of non-conduction. When a forward voltage V_{DS} is applied between the drain and the source, the PN junction between the P-body and the N-type drift region will tolerate the drain-source voltage in this condition [10]. When V_{DS} increases to the point where the PN junction breaks down, the drain-source current I_{DS} increases sharply, and the device enters avalanche breakdown, known as the breakdown voltage BV .

When V_{GS} is greater than V_{th} , the device turns on. In this state, electrons and holes in the P-body move under the influence of the electric field, forming an inversion conduction channel, enabling the movement of electrons from the source to the drain due to the effect of V_{DS} .

Due to its excellent properties, 4H-SiC is ideal for application in MOSFETs. The 4H-SiC material has a wide bandgap of 3.26 eV, enables it to operate at high temperatures without generating excessive thermal electrons. Its high breakdown electric field (2.5×10^6 V/cm) allows the device to operate at high voltages without easily breaking down. Additionally, The thermal conductivity of 4H-SiC is 4.9 W/(cm·°C), means it can effectively dissipate heat, improving the device's stability and reliability.

In a 4H-SiC MOSFET, the source, drain, and gate correspond to the current's entry, exit, and control terminals, respectively. The gate voltage governs the formation of an inversion layer, thereby regulating the current flow between the drain and source. The current flowing between the drain and source is primarily determined by the concentration and mobility of carriers in the drift region. These factors also influence the device's resistance.

3.2. Compares the Planar (VDMOS) and Trench (TMOS) structures.

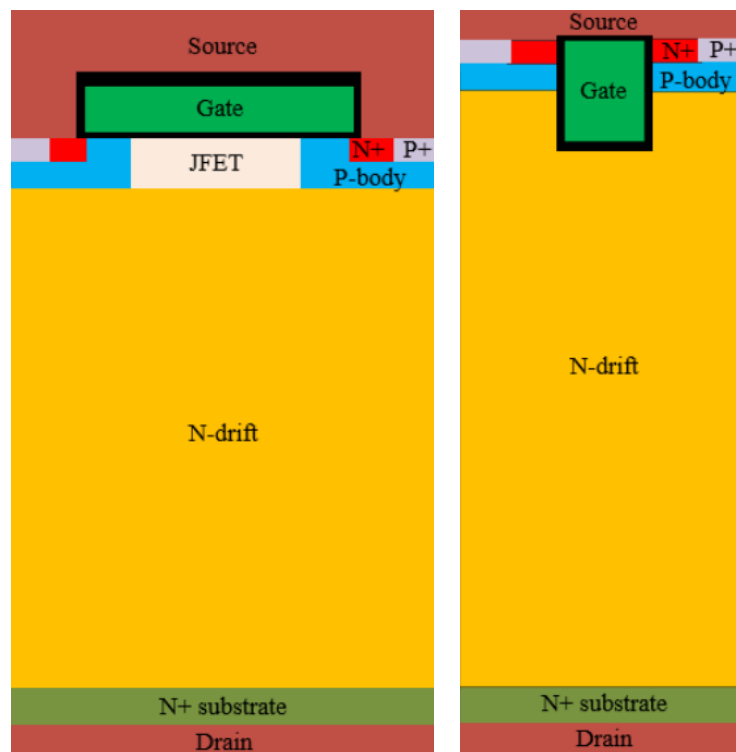


Figure 1. (Left) Planar SiC MOSFET. (Right) Trench SiC MOSFET structures [11].

3.2.1. Planar (VDMOS)

As shown in Figure 1, the planar MOSFET structure is relatively simple. The semiconductor's surface hosts the gate and electrodes. An oxide layer separates the gate from the semiconductor material, creating isolation. When a gate voltage is applied, an electric field acts on the semiconductor surface, forming an inversion layer. The advantage of the planar structure lies in its relatively simple process, making it easy to manufacture and integrate [12]. However, the planar MOSFET also has its disadvantages, primarily its higher on-resistance. This is because the current encounters significant resistance when passing through the JFET region and the drift region. Planar MOSFETs perform well in low-voltage and medium-power applications. However, their performance in high-voltage applications is inferior to trench MOSFETs due to higher on-resistance and lower carrier mobility [13].

3.2.2. Trench (TMOS)

As shown in Figure 1, the design of trench MOSFETs aims to improve current conduction capability and reduce on-resistance. Its structure involves etching vertical trenches into the semiconductor material and depositing the gate oxide layer and gate material within these trenches. This allows the gate voltage to more effectively control the current path within the trench, thereby reducing the resistance along the current path [14].

The main advantages of trench MOSFETs are their higher channel mobility and lower on-resistance. Given the current vertical control of the path, the trench structure enables a more efficient utilization of the gate voltage in order to establish a conductive channel. In addition, the trench structure has the ability to decrease the resistance of the drift region, resulting in a substantial reduction in the overall on-resistance.

Trench MOSFETs perform excellently in high-voltage, high-power applications. However, due to their complex structure, the manufacturing process requirements are higher, especially in the etching of trenches and the deposition of gate materials, which require precise control. This makes the production cost of trench MOSFETs relatively high, but their superior performance makes this cost worthwhile.

4. Design of High-Voltage 4H-SiC MOSFET Devices

4.1. Key Design Parameters and Optimization

Figure 2 displays the schematic diagram illustrating the cell structure of a 4H-SiC MOSFET. The N-type epitaxial material's thickness and doping concentration, as well as the P-base doping distribution, gate oxide thickness, width of the JFET region, and channel length, significantly impact the device's performance. N-Type Epitaxial Layer Design.

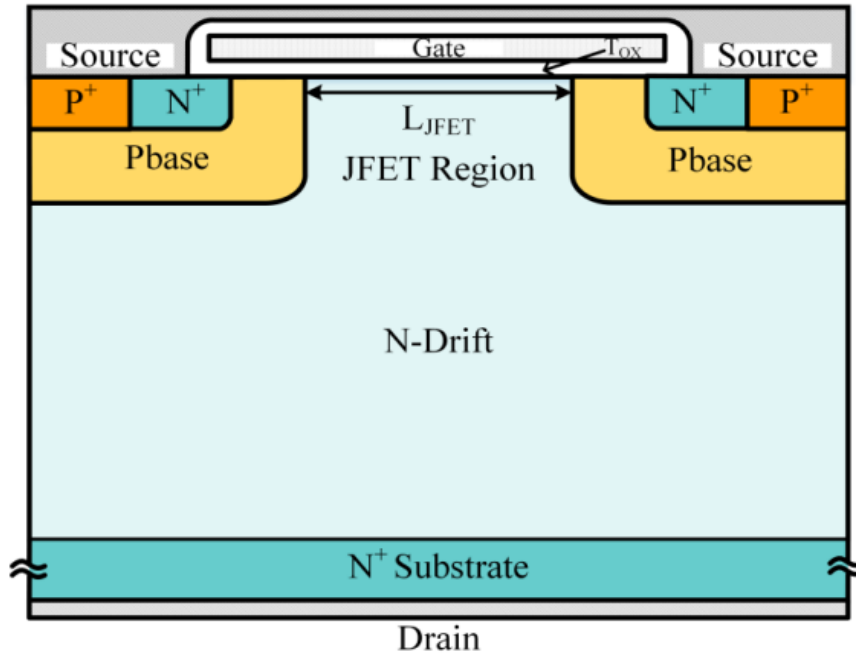


Figure 2. 4H-SiC MOSFET Cell Structure Diagram [3].

Choosing the right thickness and doping concentration of the drift region (epitaxial layer) is crucial for ultra-high voltage 4H-SiC MOSFETs. Selecting appropriate epitaxial parameters is essential to provide a foundation for subsequent terminal structure design and wafer fabrication experiments. These parameters directly affect the MOSFET's on-resistance and breakdown voltage. The simulation results indicate that the thickness of the drift region, ranging from $90\mu\text{m}$ to $110\mu\text{m}$, and the doping concentration, ranging from $4 \times 10^{14} \text{ cm}^{-3}$ to $6 \times 10^{14} \text{ cm}^{-3}$, have a substantial influence on the breakdown voltage [3]. For instance, when the doping concentration is $5 \times 10^{14} \text{ cm}^{-3}$, the breakdown voltages at various thicknesses are as follows: 12928V at $90\mu\text{m}$, 14000V at $100\mu\text{m}$, and 14992V at $110\mu\text{m}$. Hence, by suitably augmenting the thickness of the drift region, one can effectively enhance the breakdown voltage. However, an excessively thick drift region can lead to a significant decrease in conduction current, so a balance must be found between breakdown voltage and conduction current.

4.2. P-Base Region Doping Distribution

The ion implantation in ultra-high voltage 4H-SiC MOSFETs includes Pbase implantation, N+ implantation, and P+ implantation. Among these, the Pbase has a significant impact on the device's blocking characteristics, threshold characteristics, and conduction characteristics. In contrast, the N+ source region and the P+ source region mainly affect ohmic contact considerations. Therefore, in the simulation of the device's blocking characteristics, the focus is primarily on optimizing the Pbase implantation conditions.

The following simulations examine Pbase doping under various implantation doses and energy conditions, labeled as A, B, C, D, E, and F. The doping profiles and corresponding breakdown voltages are shown in Table 1. The breakdown voltage data measured in the experiments are as follows:

Table 1. Simulation Parameters for Different Doping Types [4].

Doping Type	Peak Junction Depth (μm)	Peak Concentration (cm^{-3})	Breakdown Voltage (V)
A	0.56	1.96×10^{18}	14000
B	0.28	2.76×10^{18}	13979
C	0.56	9.3×10^{17}	13237
D	0.28	1.35×10^{18}	11790
E	0.56	2.79×10^{16}	246
F	0.56	2.03×10^{19}	14000

The experimental results indicate that doping types A and F can ensure high breakdown voltage while providing optimal threshold voltage and conduction current. Specifically, Type A doping achieved a conduction current of 200 A/cm^2 at a gate voltage of 10V , whereas Type F doping reached 220 A/cm^2 . However, due to the higher peak concentration of Type F doping, it may increase manufacturing costs. Therefore, Type A doping was ultimately chosen as the optimal doping scheme.

4.3. Gate Oxide Layer Thickness

The thickness of the gate oxide T_{ox} exerts a substantial influence on the performance of the device. The gate oxide thickness is the measurement of the thickness of the oxide layer that separates the gate from the semiconductor in a MOSFET. The gate is the electrode that controls the flow of current, while the oxide layer (usually silicon dioxide, SiO_2) serves as an insulator. On one hand, increasing the thickness of the gate oxide reduces the capacitance of the gate oxide layer, which in turn increases the threshold voltage (the minimum voltage required to turn on the MOSFET) and decreases the device's conduction capability. On the other hand, decreasing the thickness of the gate oxide layer increases the electric field strength across it when the device is in a reverse blocking state, thereby diminishing the reliability of the gate oxide. The reverse blocking state refers to when the MOSFET prevents current from flowing through it when a reverse voltage is applied. This is especially critical for 4H-SiC (4H-type silicon carbide) MOSFETs, as the critical breakdown field of 4H-SiC is close to that of SiO_2 . Therefore, the gate oxide thickness for 4H-SiC MOSFETs needs to be thoroughly optimized through simulation. To balance these factors, an appropriate oxide layer thickness must be chosen. Experiments were carried out to confirm and analyze the influence of varying gate oxide thicknesses on the performance of the device. In order to accomplish this, devices with gate oxide thicknesses of 20 nm , 40 nm , 60 nm , and 80 nm were subjected to testing. The obtained experimental results are presented in Table 2 below:

Table 2. Impact of Gate Oxide Thickness on SiC MOSFET Parameters [4].

Gate Oxide Thickness (T_{ox})	Threshold Voltage (V)	Conduction Current (A/cm^2)	Gate Oxide Reliability (MV/cm)
20 nm	1.4	250	3.2
40 nm	2.8	230	2.5
60 nm	4.1	220	2.0
80 nm	5.5	200	1.6

From the experimental results, it can be seen that as the gate oxide thickness increases, the threshold voltage significantly increases. Additionally, the conduction current slightly decreases [15]. Furthermore, the reliability of the gate oxide improves with increased thickness [16]. Considering all factors, a gate oxide thickness of 60 nm was ultimately chosen. This thickness ensures device reliability while providing good conduction performance.

4.4. Gate Oxide Reinforcement Structure Design

In order to enhance the dependability of 4H-SiC MOSFETs, a gate oxide reinforcement structure design is proposed. The design incorporates trench etching and implantation in the JFET region to mitigate the electric field intensity on the gate oxide layer [14]. Simulation optimization results show that by adjusting the size of the JFET region implantation window, trench depth, and overall width of the JFET region, the breakdown voltage and reliability of the device can be significantly improved.

5. Conclusion

This study focuses on investigating the design and optimization of high-voltage 4H-SiC MOSFET devices, with a particular emphasis on their notable benefits in applications that involve high temperatures, high frequencies, and high power. By conducting a thorough examination of the characteristics of 4H-SiC materials, this paper has determined that their significant bandgap, high breakdown electric field, and excellent thermal conductivity make them highly promising for various applications in the realm of power electronics. Globally, numerous companies have achieved substantial advancements in the research of 4H-SiC MOSFET devices. Although domestic research has mainly focused on the 600V to 1700V range, notable achievements have also been realized.

This study uses simulation software such as Silvaco to optimize the design parameters of high-voltage SiC MOSFETs, including P-base doping distribution, gate oxide thickness, and JFET region length. The introduction of multi-zone modulation field limiting ring technology has significantly enhanced the breakdown voltage of the devices. Additionally, by comparing planar (VDMOS) and trench (TMOS) structures, this paper found that trench structures have lower on-resistance and higher carrier mobility in high-voltage, high-power applications, albeit at a higher manufacturing cost.

Looking forward, 4H-SiC MOSFET devices show great potential in several emerging fields. For example, in electric vehicles, SiC MOSFETs can significantly improve power conversion efficiency, reduce energy loss, and thus extend battery life and driving range. SiC MOSFETs play a crucial role in improving energy conversion efficiency and lowering system costs in renewable energy industries like photovoltaic inverters and wind power systems due to their high efficiency and reliability. Moreover, in aerospace, SiC MOSFETs are widely used in the power systems of satellites and spacecraft due to their stability in high-temperature and high-radiation environments.

In conclusion, this study establishes a theoretical foundation and improvement for the design and optimization of SiC MOSFET devices in high-voltage, high-power, and emerging applications, heralding significant advancements in power electronic device technology and its widespread application. These findings not only promote the further development of SiC technology but also lay the groundwork for achieving more efficient and reliable power conversion.

References

- [1] J.W. Palmour, R. Singh, J.A. Edmond, C.H. Carter Jr. (1995) Silicon Carbide Power Devices. World Scientific Publishing, Singapore.
- [2] M. Bhatnagar, B.J. Baliga, Analysis of silicon carbide power device performance, 3rd International Symposium on Power Semiconductor Devices and ICs, Baltimore, MD, 1991.
- [3] B.A. Hull et al., Status of 1200V 4H-SiC Power DMOSFETs, 2007 International Semiconductor Device Research Symposium, College Park, MD, 2007.
- [4] Ben Tan, Research on the Design and Key Technology of Ultra-high Voltage 4H-SiC MOSFET Devices, Master's thesis, University of Electronic Science and Technology of China, 2019.
- [5] E.V. Brunt, L. Cheng, M. O'Loughlin, C. Capell, C. Jonas, K. Lam, et al., 22 kV, 1 cm², 4H-SiC n-IGBTs with Improved Conductivity Modulation, 26th International Symposium on Power Semiconductor Devices & ICs, Waikoloa, Hawaii, 2014.
- [6] R. Nakamura, Y. Nakano, M. Aketa, K. Noriaki, K. Ino, 1200V 4H-SiC Trench Devices, PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, 2014.

- [7] A. Agarwal, S.H. Ryu, J. Palmour. (2004) Power MOSFETs in 4H-SiC: Device design and technology. Springer, Berlin.
- [8] Yuming Zhang, Xiaoyan Tang, Qingwen Song, Research Status of Silicon Carbide Power Devices, *New Mater. Ind.* 10 (2015) 26-30.
- [9] Y.J. He, Design and key process research of high-performance 4H-SiC power VDMOSFET devices, Xi'an University of Electronic Science and Technology, 2018.
- [10] M. Bhatnagar, B.J. Baliga, Comparison of 6H-SiC, 3C-SiC, and Si for power devices, *IEEE Trans. Electron Devices* 40 (1993) 645-655.
- [11] Wei Tan, Electrical reliability study of 1200 V 4H-SiC MOSFETs, Jiangnan University, 2024.
- [12] S.M. Sze, Kwok K. Ng. (2006) *Physics of Semiconductor Devices*. Wiley-Interscience, Victoria.
- [13] S. Zhu, T. Liu, J. Fan, H.L.R. Maddy, M.H. White, A.K. Agarwal, Effects of JFET Region Design and Gate Oxide Thickness on the Static and Dynamic Performance of 650 V SiC Planar Power MOSFETs, *Mater.* 15 (2022) 17.
- [14] Darwish, Mohamed N. et al. "A new power W-gated trench MOSFET (WMOSFET) with high switching performance." *Proceedings of the 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs (ISPSD '03)*, (2003) 24-27.
- [15] Laura Anoldo, Edoardo Zanetti, Walter Coco, Alfio Russo, Patrick Fiorenza, Fabrizio Roccaforte, 4H-SiC MOSFET Threshold Voltage Instability Evaluated via Pulsed High-Temperature Reverse Bias and Negative Gate Bias Stresses, *Mater.* 17 (2024) 1908.
- [16] Materials, Free Full-Text, The Influence of Special Environments on SiC MOSFETs, *Mater.* 16 (2024) 18.