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Optimization design and application scenario research of low power digital integrated circuit

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Abstract. This paper explores the importance of low-power digital integrated circuits (IC) in technological development and everyday applications, especially their key role in modern electronic devices such as smartphones and advanced medical devices. With the advent of the digital age, the design efficiency and energy efficiency of low-power IC have a direct impact on device performance and sustainability. Based on the design basis of low power IC, CMOS technology and its power consumption model are discussed in detail, and dynamic and static power consumption is reduced by means of dynamic voltage frequency regulation, multi-threshold CMOS technology and clock gating technology. In addition, the paper explores in depth the verification and optimization process of low-power designs, emphasizing the importance of experiments and simulations in accurately evaluating and adjusting power consumption. Finally, the paper focuses on the key applications of low-power design in mobile devices and medical devices and presents some practical application cases. The research in this paper will help to promote the wide application of low-power IC in different fields and contribute to scientific and technological progress and social needs.

Keywords: Low power; digital integrated circuits; CMOS technology; dynamic voltage-frequency; multi-threshold.

1. Introduction

With the advent of the digital age, low-power digital integrated circuits (IC) are playing an increasingly important role in technology development and daily applications. These integrated circuits are an integral part of modern electronic devices, from smartphones to advanced medical devices, and their efficient and low-energy design has a direct impact on the performance and sustainability of the device [1]. Therefore, exploring the design principles, technical challenges, and their practical applications in various fields of low-power IC is crucial to driving technological progress and meeting societal needs.

Based on the design basis of low power IC, this paper discusses CMOS technology and its power consumption model in detail, and how to reduce dynamic and static power consumption through dynamic voltage-frequency regulation (DVFS), multi-threshold CMOS technology and clock gating technology. Further, we explore the verification and optimization process of low-power designs, emphasizing the importance of experiments and simulations in accurately evaluating and adjusting power consumption. Finally, the paper focuses on the key applications of low-power design in mobile devices and medical devices, revealing some examples of the potential of these technologies to promote device portability, extend battery life, and reduce healthcare costs.

Through this comprehensive analysis, this paper not only provides an opportunity for in-depth understanding of low-power digital integrated circuit design, but also highlights the importance of technological innovation and future development trends in this field, demonstrating its great value and potential in practical applications.

2. Design basis and research analysis of low-power digital integrated circuits

2.1. CMOS technology and power consumption model

CMOS (Complementary metal oxide semiconductor) technology is at the heart of modern digital integrated circuits (IC) and is widely used to manufacture microprocessors, memory, and other digital logic chips in various electronic devices. CMOS technology is popular mainly because of its low power consumption, high noise tolerance, and large-scale integration capabilities. The technology is based on complementary combinations of N-type and P-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to perform logic functions. The N-type transistor conducts electricity at logic "1", while the P-type transistor conducts electricity at logic "0", and this configuration ensures that both do not conduct electricity at the same time in the steady state, thus significantly reducing static power consumption [2].

At the same time, with the rapid development of microelectronics technology, the function of integrated circuits is becoming more and more powerful, the size of transistors is shrinking, and the power consumption problem of CMOS technology begins to appear and become the key challenge of design. Power consumption not only affects battery life, but also causes thermal problems and reduces the reliability and life of integrated circuits. Therefore, energy consumption in CMOS circuit design can be accurately evaluated and optimized by power consumption model. The power consumption of CMOS circuits is mainly divided into two categories: dynamic power consumption and static power consumption. Dynamic power consumption is generated when the transistor is switched on and off, mainly due to the capacitor effect during the charge and discharge process. Because the dynamic power consumption is proportional to the square of the switching frequency and voltage, reducing the voltage and frequency is one way to control the dynamic power consumption. The static power consumption is mainly caused by the transistor leakage current, and due to the characteristics of modern processes; this situation becomes more serious in micro-sized transistors. It often includes subthreshold leakage current, gate leakage and source-drain junction current. Static power consumption can be reduced by improving the process, optimizing the transistor design, and using low-power technologies [3].

2.2. Common power consumption reduction technologies

In order to achieve low power design, it is very important to adopt the appropriate technical strategy. In the design of digital integrated circuits, the common power consumption reduction methods include clock gating, Dynamic Voltage Frequency Regulation (DVFS), multi-threshold CMOS technology, memory element optimization and power allocation. Considering that the power consumption is proportional to the square of the voltage, the dynamic power consumption can be effectively reduced by reducing the voltage and frequency when the processor is idle or the load is low. DVFS is a widely used energy saving technology in processor design, especially in mobile and portable devices, to help extend battery life and reduce heat generation.

Clock gating technology can effectively reduce energy consumption when logic idle, it reduces energy consumption by turning off the clock of the circuit that is not processing data. The reduction of the supply voltage can significantly reduce the energy consumption caused by charge pumping. However, this can also have a negative impact on the speed of the circuit, so designers need to find a balance between speed and power consumption [4].

Multi-threshold CMOS (MTCMOS) technology is a method of using transistors with different threshold voltages in the design. The higher the threshold voltage of the transistor, the smaller the leakage current. MTCMOS technology uses a combination of high threshold voltage (HVT) transistors and low threshold voltage (LVT) transistors. High-threshold transistors help reduce static power when the IC is idle, while low-threshold transistors are used in critical paths that require fast switching, ensuring performance while reducing dynamic power [5]. Therefore, the power reduction of IC design is a complex and multi-dimensional task, which requires the comprehensive use of

various strategies and technologies. From static power management to dynamic power management strategies to innovative MTCMOS technology, designers must carefully balance power consumption and performance so that they can design circuits with lower power consumption to achieve higher performance.

2.3. Low power design verification and optimization

Even if the strategy of reducing power consumption is adopted in the design stage, if it does not pass the subsequent verification and optimization, it is still impossible to ensure that the realized circuit meets the requirements of low power consumption. Therefore, after the design is completed, accurate power evaluation and necessary optimization adjustments are essential. In the process of verification and optimization, we can define the basic parameters, establish the power consumption model, and then verify and optimize the circuit design repeatedly through experiments. According to the research process of Liu Jian et al., it can be seen that they can modify the software of the wireless sensor intelligent node, set different WDT and ODC parameters, and carry out several experiments to get the actual power, and compare it with the power consumption obtained by the theoretical model under the same parameters. In order to obtain more accurate results [6].

At the same time, modern EDA tools can simulate circuit performance at different temperatures and voltages, helping engineers find the most energy-efficient combination of design parameters. For example, in the design and physical implementation of low-power gate level circuits, static and dynamic power consumption of deep submicron processes are considered, frequency hopping and leakage are optimized by different threshold voltage standard units, and EDA tools are iteratively designed to meet performance and power requirements [7]. The final method of specific verification and optimization can also be verified by using a variety of different operating conditions and power test results. In-depth analysis of power management module design or in the design process, standard units with different threshold voltages are used to balance power consumption and performance to improve the design of integrated circuits.

3. Low power digital integrated circuit application field

3.1. Low power design in mobile devices

In today's mobile era, power consumption has become one of the key factors limiting the performance and functionality of mobile devices. With the gradual development of mobile devices towards smaller and more intelligent, the requirements for low power consumption of integrated circuits are increasingly stringent. The portability and continuous operating time capabilities of electronic devices depend heavily on the efficient, low-energy design of their internal integrated circuits. I believe that low-power IC design should be the focus of research and development, and successful low-power IC design should consider the system requirements and power efficiency and use innovative technologies to minimize the energy consumption of the circuit, while ensuring that performance is not affected.

In the paper of Zhao Hongliang et al, they present a low-power low-temperature readout integrated circuit (ROIC) designed for a 512×512-pixel Infrared focal plane array (IRFPA) [8]. To improve the accuracy of circuit simulation at low temperature, an improved MOS device model is proposed based on BSIM3 model, and correction parameters are introduced to describe the carrier freezing effect at low temperature, thus improving the fitting accuracy of low temperature MOS device simulation. In addition, they used a capacitor-resistive amplifier (CTIA) with an inherently correlated double sampling (CDS) configuration for high-performance readout interface circuits. The paper reduces power consumption by using optimized readout timing and structure, achieving a readout rate of more than 10 MHz while keeping power consumption below 70 milliwatts. This case shows that through technological innovation and clever design, the goal of low-power circuits can be achieved even in harsh working environments.

Based on a research paper by Toyozawa et al. [9], they developed a 2.2-inch 176x(RGB)x220 pixel Poly-Si TFTs reflective LCD for mobile device applications. The display uses a low power consumption level shifter system and a highly efficient DC-DC converter, which are integrated on a glass substrate using poly-Si TFTs, reducing the power consumption of the LCD panel to 0.87 mW. It is worth mentioning that the power consumption of this device is 43% lower than the previous technology. This demonstrates the outstanding benefits of LTPS TFT circuit technology, which can significantly reduce power consumption even in full-screen display mode.

In the design aspect, the peripheral circuit can be optimized by controlling the N-type and P-type transistors respectively, and the goal of low power consumption and high performance can be achieved. For example, Wang et al. studied the SRAM macro design for mobile applications under the 65nm ultra-low power CMOS technology [10]. Using technologies such as programmable nMOS sleep bias transistors, floating bit line, and SRAM pMOS reverse body bias, they achieved the goal of a 1Mb SRAM macro leak current of less than 20μA in standby mode, while maintaining support for the 1.1GHz operating frequency required for rich multimedia applications. The 65 nm strain silicon technology used excelled in both improving transistor performance and reducing leakage, demonstrating that high-speed memory design can be achieved through advanced design strategies even under the constraints of ultra-low power consumption.

3.2. Low power circuit design in medical devices

In today's medical field, with the popularity of implantable medical devices, the need for low-power integrated circuit design has become increasingly urgent. These devices tend to run for long periods of time and are not easy to charge or replace batteries frequently. Therefore, low-power circuit design not only optimizes the battery life of the device, but also reduces patient interference and medical costs. I think low power IC design in implantable medical devices, efficient energy conversion circuits and power minimization controllers are key.

For implanted medical devices, Yaoyao Jia and other collaborators describe progress in this regard in a paper published in IEEE Journal, specifically regarding the implementation of a low voltage CMOS process for adaptive power supply for implantable biomedical applications [11]. And wireless power transmission technology for pose and orientation insensitive of the Ener-Cage-Homecage system. This confirms that the use of low-power integrated circuits in the design of implantable medical devices is a key factor in ensuring the efficient and reliable operation of such devices.

In implanted medical devices, the design of efficient energy conversion circuit is the key. For example, Lee et al. demonstrated in their paper a novel leakage reduction technique to achieve efficient conversion of RF signal to DC voltage [12]. In addition, the research also proposes a linear regulator with low static current and a BPSK demodulator and CDR circuit based on CDS technology, which are essential to ensure low power operation and signal stability. This relatively low data transmission rate reduces the energy consumption of the system and ADAPTS to the needs of medical devices for bio signal processing.

In addition to efficient energy conversion, minimizing energy consumption is also a key means to achieve low power consumption. Laouej et al. 's paper showcases a concrete example designed for biomedical applications with the proposed incremental Delta-σ modulator [13]. With TSMC CMOS technology, the designed circuit consumes only 3 μW of power at ±0.5 V supply voltage. It can handle input signals of -1.93 dBFS size and 68.66 kHz frequency, which shows that this design solution achieves extremely low power consumption while maintaining a high signal-to-noise ratio and good resolution.

4. Conclusion

This paper comprehensively explore the design principles, technical challenges, and far-reaching implications of low-power digital integrated circuits in key areas. Through in-depth analysis of the power consumption model of CMOS technology, combined with advanced methods such as dynamic

voltage-frequency regulation (DVFS), multi-threshold CMOS technology and clock gating technology, this paper reveals how to effectively reduce the dynamic and static power consumption of integrated circuits to achieve efficient and sustainable electronic product design.

With the continuous advancement of technology, low-power design not only shows its importance in fields such as mobile devices and medical devices, but also its contribution to reducing environmental impact, improving device performance and extending battery life. By adopting low-power technologies, we are able to advance innovation in electronic devices to meet growing market demands and more stringent environmental standards.

Looking forward to the future, with the continuous emergence of new materials, new processes and new technologies, the design and application of low-power digital integrated circuits will usher in broader prospects for development. From microelectronics to nanoelectronics, from Earth to space, the innovation and application of low-power technologies will continue to promote the development of electronic devices in the direction of higher performance, more environmentally friendly and more intelligent. Therefore, strengthening the research on low-power integrated circuits is not only an important task in the field of electronic engineering, but also a key way to achieve the sustainable development goals and build a better future.

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