WEP Warwick Evans Publishing

International Journal of Materials Science and Technology Studies

ISSN: 3006-7693 (Print), ISSN: 3006-3744 (Online) | Volume 5, Number 3, Year 2026
DOI: https://doi.org/10.62051/ijmsts.v5n3.03
Journal homepage: https://wepub.org/index.php/IJMSTS/index

Functional Integration and Performance Optimization of Semiconductor Chips and Integrated Circuits in Smart Electronic Devices

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ABSTRACT

In order to clarify the functional integration modes and performance optimization directions of semiconductor chips and integrated circuits in smart electronic devices, this paper combines the 2024-2025 measured industrial data of the semiconductor industry to sort out the development history of chip integration technologies, analyze the practical roles of SoC (System on Chip) and Chiplet architectures in functional integration, explore the improvement effects of low-power design, advanced packaging and new materials on chip performance, and summarize the design concepts for the collaborative optimization of chip functionality and performance. Research indicates that by 2025, high-end advanced packaging has become the core technical support for heterogeneous chip integration; the shipment volume of advanced-process high-end SoCs for smartphones continues to rise. Chiplet and high-density interconnect (HDI) technologies can effectively improve the functional integration density of chips, and relevant technological innovations have continuously broken through the performance limitations of traditional silicon-based processes. The optimization strategies summarized in this paper based on practical industrial applications can provide feasible practical references for the design and performance upgrading of chips used in smart electronic devices.

KEYWORDS

Semiconductor chips; Integrated circuits; Smart electronic devices; Functional integration; Performance optimization; Advanced packaging; Low-power design

1. INTRODUCTION

Artificial intelligence, the Internet of Things, and mobile communication technologies continue to popularize, and various intelligent electronic devices such as smartphones, wearable devices, and smart homes are constantly upgrading towards lightweight, low-power, and multifunctional directions. Chips and integrated circuits, as the core hardware of smart devices, must feature high integration, low power consumption, and high computing power in order to meet the practical needs of device miniaturization, long battery life, and high performance. The traditional design method of combining discrete components is no longer suitable for the development requirements of the new generation of intelligent terminals. Therefore, the integration of chip functions and performance improvement have become an important direction for industry technological development.

In 2025, the global semiconductor industry has entered a critical period of technological upgrading, with significant breakthroughs in advanced processes and packaging technologies, and chip architectures are gradually shifting to heterogeneous integration. In terms of functional integration, SoC chips integrate computing, communication, image processing and other functional modules,

which has become a common solution in the industry. Chiplet architecture breaks through the physical limitations of single-chip integration and can efficiently integrate chips from different processes. In terms of performance improvement, dynamic power management and advanced packaging technology have been improved from both circuit design and physical structure aspects, which can effectively reduce chip power consumption and enhance overall computing capability.

According to data from CounterPoint Research, by 2025, the proportion of shipments of 5nm and more advanced processes in global smartphone AP SoC chips has reached 51%, breaking through half for the first time [1]. At the same time, the proportion of advanced packaging applications in AI chips and high-end terminal devices continues to rise, and technologies such as hybrid bonding and 3D stacking are gradually being applied on a large scale, further improving the integration and energy efficiency performance of chips. This article combines industry cases and authoritative data to conduct research from five perspectives: architecture, power consumption, packaging, materials, and collaborative design, providing reference for the engineering implementation of chip function integration and performance improvement.

2. THE MAINSTREAM ARCHITECTURE EVOLUTION OF INTELLIGENT ELECTRONIC DEVICE CHIP FUNCTION INTEGRATION

Intelligent electronic devices have multiple usage scenarios, driving chip architectures to evolve from discrete designs to systematic and integrated solutions. SoC and Chiplet are currently the main technical methods for achieving functional integration, which are suitable for different levels of terminal products and together form a technology system for chip functional integration.

Among them, SoC system level chips are the main integration solution for consumer intelligent electronic devices. They integrate functional units such as CPU, GPU, ISP, and baseband on a single die, and can simultaneously handle multiple tasks [2]. Flagship SoC can integrate multiple functional modules to meet the needs of 4K video processing, 5G communication, and end-to-end AI inference. Mid-to-low-end smart bracelets and IoT terminals adopt simplified SoCs, focusing on core functions such as sensing and communication, with stable low-power operation and cost-effectiveness that match product positioning. For example, the Xiaomi Xuan Jie O1 processor adopts 3nm technology, with a chip area of 109 mm^2, 19 billion transistors, integrated ten core four cluster CPU and multiple functional modules, and an AnTuTu benchmark score of over 3 million.

Chiplet technology is mainly used for high-end intelligent devices, resolving the high manufacturing cost and single-chip integration challenges of advanced processes. This technology connects chips with different processes and functions through packaging technology, allowing for flexible combination of functional modules. According to actual testing by Xinyuan Microelectronics, the use of Chiplet technology can shorten ASIC development time by 30%–50%, reduce manufacturing costs by 20% -40%, and improve the flexibility of functional expansion.

In addition, the compute-in-memory (CIM) architecture is mainly used in AI computing scenarios for intelligent terminals, which can improve data processing efficiency. The traditional von Neumann architecture suffers from the problem of separation of storage and computation, which consumes a large amount of power when transferring data. The integration of storage and computation combines computing and storage units to reduce data migration losses [3]. Research conducted by the Institute of Microelectronics of the Chinese Academy of Sciences in 2024 shows that SRAM-based in-memory computing chips have significantly improved energy efficiency and computing power compared with traditional architectures. The edge AI chips launched by multiple domestic chip manufacturers all adopt SRAM-based compute-in-memory (CIM) design. In devices such as smart cameras and voice assistants, the inference power consumption is reduced by more than 60% compared to traditional architectures. Zhicun Technology WTM2101 is the world's first NOR Flash based compute-in-

memory voice chip, with a power consumption of only 5 mW, which increases computing power by 10 to 200 times compared to traditional platforms under the same power consumption.

3. LOW POWER PERFORMANCE IMPROVEMENT TECHNOLOGY PATH FOR INTELLIGENT ELECTRONIC DEVICE CHIPS

Power consumption control is the core indicator for optimizing the performance of intelligent electronic device chips, especially for battery-powered mobile terminals. While ensuring computing power, power consumption reduction has long been a core industry focus. Based on this demand, the industry has gradually built a complete low-power optimization technology system from four levels: architecture, circuit, process, and system.

The optimization at the architecture level is centered around dynamic power regulation, and the long-term validated Dynamic Voltage Frequency Regulation (DVFS) technology has become the mainstream solution. The chip can dynamically adjust operating voltage and frequency based on real-time load, and lower the operating parameters in light load state to reduce ineffective power consumption. Experimental data shows that the standby power consumption of mobile SoC equipped with this technology can be reduced by about 70%. Combined with multi-power-domain partitioning technology, it can also separately power off idle modules, making energy efficiency control more precise [4].

In addition to architecture control, the optimization of circuit design also provides support for power consumption control from the bottom layer. Approximate computing is suitable for scenarios such as image processing and speech recognition that are less sensitive to computational accuracy. It uses low bit width integer operations instead of traditional floating-point operations, which can reduce computational power consumption by over 50% while maintaining performance loss outside the user's perceptible range [5].

According to publicly available data from TSMC (2024), 3nm process chips can reduce power consumption by 25% -30% and increase integration by 20% compared to the 5nm version under the same performance. The Xiaomi Xuan Jie O1 chip also adopts refined layout and ultra-low voltage design on this basis, achieving an optimal balance between computing performance and power efficiency via precise tuning.

The low-power optimization effect of chips cannot be achieved without collaborative adaptation with terminal systems. Chip manufacturers will customize power consumption strategies based on the actual usage scenarios of the devices. For example, smartwatches will automatically switch to low-power mode in low-frequency scenarios such as heart rate monitoring and off-screen display. The underlying power consumption scheduling of Android and iOS systems is also deeply adapted to the chip hardware. The Apple A18 Pro chip, when adapted to iOS 18, has a comprehensive battery life increase of 23%, which is a typical result of software-hardware collaboration. Low power optimization is not simply sacrificing performance, but achieving a balance between computing power and energy consumption through fine tuning. This multi-level optimization solution can also better meet the power consumption needs of different intelligent electronic devices.

4. THE ROLE OF ADVANCED PACKAGING TECHNOLOGY IN IMPROVING CHIP INTEGRATION AND PERFORMANCE

Advanced packaging technology, as a key connecting carrier between chip design and terminal applications, has broken through the traditional function of physical protection. It has become the core support for improving chip performance in the post-Moore era, relying on heterogeneous integration to overcome the single-chip integration bottleneck and provide a key path for the leap of AI and high-performance computing power.

2.5D packaging is the mainstream solution for high-end intelligent chips, which achieves high-density interconnection of multiple chips through a silicon interposer and reduces signal transmission latency. TSMC CoWoS packaging has been widely adopted in high-performance terminal chips. Compared with traditional packaging, signal delay is reduced by 40%, and interconnect density is increased by three times. It can efficiently integrate SoC and HBM, enhance data throughput capability, and adapt to high-definition video, AI computing and other scenarios. The NVIDIA H100 GPU leverages this packaging to deliver TB/s-class bandwidth, becoming the core computing power unit for AI training [6].

3D packaging improves integration density and reduces volume by vertically stacking chips, and achieves multi-layer chip interconnection through TSV silicon vias, catering to the stringent spatial requirements of AR/VR and micro-wearable devices. According to Yole Group's 2025 data, the volume of 3D packaged chips has been reduced by 70%, and the heat dissipation efficiency has been improved by 40%, solving the problem of high-density integrated heat dissipation. Intel Foveros Direct technology optimizes stacking accuracy, and its 3D server chips rely on heterogeneous integration to significantly improve performance density.

Fan-out packaging balances performance and cost, and is widely used in mid-to-high-end mobile terminals and smart home appliance chips. This technology abandons traditional substrates, achieves pin fan-out, reduces packaging size, and optimizes heat dissipation. According to QYResearch's 2024 data, its consumer electronics penetration rate reached 36.3%, reducing BGA packaging costs by 20% and power consumption by 12%. The Apple iPhone processor adopts InFO PoP packaging, significantly reducing thickness and enabling terminal lightweight design.

SiP system-level packaging can integrate chips, passive components, and sensors, achieving "package as system" and widely used in micro-wearable devices. It integrates multifunctional modules and suppresses signal interference within miniaturized volumes. The Apple Watch was the first to apply this technology on a large scale in 2014, followed by AirPods to promote the iteration and upgrading of wearable devices [7].

Advanced packaging is centered around high-density interconnection and heterogeneous integration, enabling multi-process chip module collaboration and breaking through the limitations of single-chip integration. By 2025, the scale of China's advanced packaging market will exceed 110 billion RMB, and SiP and 2.5D/3D packaging will grow rapidly, becoming the core driving force for industry development.

5. PRACTICAL APPLICATION OF NEW SEMICONDUCTOR MATERIALS IN CHIP PERFORMANCE OPTIMIZATION

The performance mining of traditional silicon-based materials is approaching the physical limit. New semiconductor materials provide new physical support for chip performance optimization from dimensions such as electronic transmission, power consumption control, and integration characteristics. Some materials have been commercialized and applied to core chips of intelligent electronic devices.

Relevant research has been reviewed and found that two-dimensional semiconductor materials are an important research direction in the post-silicon-based era. Molybdenum disulfide, indium selenide, and other materials have high electron mobility and low leakage characteristics, which can be used for the preparation of low-power transistors [8]. The research conducted by the research team from Peking University shows that the average electron mobility of two-dimensional indium selenide transistors reaches 287 $cm^2/(V \cdot s)$, with a peak value of 347 $cm^2/(V \cdot s)$ and a subthreshold swing of 67.3 mV/dec, and energy consumption reduced to one-third of silicon-based devices. To some extent, it is suitable for the low-power requirements of wearable and IoT terminals. Currently, this material

is still in the early stage of industrialization and is mostly integrated with silicon-based materials to promote applications.

Gallium nitride (GaN) has been commercially used in power management chips for wide bandgap semiconductors. Its high breakdown electric field and high energy efficiency make it suitable for smart terminal fast charging and power management modules. Actual test data shows that the conversion efficiency of GaN-based power chips reaches 96.5%, and the volume is reduced by 60% compared to silicon-based solutions. It is widely used for fast charging of laptops and mobile phones, and also reduces chip heat loss.

Silicon carbide (SiC) is commonly used in smart automotive electronic chips to improve power device stability and energy efficiency. SiC MOSFET switching losses are reduced by 70% -80% compared with silicon-based IGBT, and the overall efficiency of electric drive systems increases from 91% -93% to 96% -97.5%. The efficiency of high-end systems exceeds 99% [9].

ReRAM (Resistive Random Access Memory) material is applied to integrated memory and computing chips, achieving zero static power consumption through non-volatile technology. The AI inference chip of Hefei Ruike Microelectronics uses this material, which can improve energy efficiency by more than three times compared to traditional chips in smart cameras and smart home devices.

Organic semiconductor materials are suitable for flexible smart terminals, and their advantages of bendability and low cost enable the production of flexible sensors and processors. The flexible driver chips from domestic manufacturers can withstand more than 40,000 bending cycles, reducing power consumption by 40% compared to silicon-based solutions. They have been used in foldable screen smartphones and flexible wearable devices.

New semiconductor materials are often integrated with silicon-based and new materials, gradually replacing traditional silicon-based devices and breaking through performance bottlenecks at the material level, providing technical directions for optimizing smart electronic device chips.

6. SYSTEM COLLABORATIVE DESIGN METHOD FOR CHIP FUNCTION INTEGRATION AND PERFORMANCE IMPROVEMENT

The integration of chip functions and performance enhancement are not independent technical links, and depend on system collaborative design to achieve an optimal balance of functionality, performance, cost, and reliability. This model has become the mainstream solution for the development of intelligent electronic device chips in the industry.

The demand-oriented design process is the core foundation of collaborative optimization. In the early stage of chip development, it is necessary to combine terminal product positioning, clarify functional requirements and performance indicators [10]. The demand for chips in smartphones, wearable devices, and smart homes varies significantly. High-end products focus on computing power and integration, while entry-level products focus on cost and low power consumption. The design team conducts scenario-based requirement analysis, reasonably divides functional modules, matches adaptation processes and packaging solutions, and reduces resource waste from over-integration. Adopting a demand-oriented approach to collaborative design can effectively shorten the R&D cycle, improve the compatibility between products and terminals, and reduce the cost of R&D trial and error.

Cross-level collaborative optimization covers the entire process of architecture, circuits, packaging, and systems. Architecture design can be coordinated with circuit technology to adjust module layout based on process characteristics; The synergy between chip design and packaging process can optimize the interconnect structure and reduce signal loss; The chip hardware and terminal system can collaborate to customize power consumption scheduling and computing power allocation

strategies. High end tablet chips utilize software and hardware collaboration to automatically switch performance modes in gaming, office, and other scenarios, balancing operational smoothness and power consumption control [11].

Multidisciplinary integration provides key support for collaborative design. Chip development requires the integration of multiple fields of technology, including integrated circuit design, material engineering, system software, and terminal structure design, to break through the design limitations of a single discipline. Flexible device chips require collaboration between material engineers and chip designers to develop bendable devices; AIoT chips require collaboration between algorithm engineers and hardware engineers to optimize computing power allocation and improve functionality and performance matching.

A verification and iteration mechanism ensures the effectiveness of collaborative design implementation. Through FPGA prototype verification, multi-physics simulation, and silicon validation and lab testing, defects and performance shortcomings can be identified during the development phase, reducing production rework. The industry-wide verification process can achieve high functional coverage, optimize integration issues in a timely manner, and enable chips to adapt to actual terminal usage scenarios.

7. CONCLUSION

Based on the above analysis, the functional integration and performance enhancement of chips and integrated circuits constitute the core support for the technological iteration of intelligent electronic devices. At present, the industry has gradually established a technical system that combines architecture innovation, power control, packaging improvement, material upgrading, and system collaboration. All technical paths are supported by real commercial cases and public industrial data, with practical and verifiable conclusions.

From the perspective of practical application effects, SoC, Chiplet, and compute-in-memory (CIM) architectures are respectively adapted to the functional integration requirements of consumer terminals, high-end devices, and AI scenarios. The combination of multiple architectures better aligns chip functions with actual terminal application scenarios. In terms of performance improvement, multi-level low-power design techniques, advanced packaging technology, and new semiconductor materials are working together to continuously optimize the energy efficiency and computing power level of chips. System collaborative design relies on demand-oriented, cross-layer optimization, and interdisciplinary integration, effectively balancing the relationship between chip functionality and performance. It not only reduces R&D costs but also improves chip-terminal product compatibility. Industry data also confirms that integration and high energy efficiency are still the core trends in chip technology development.

Currently, various new technologies are still being implemented through the integration of silicon-based and new materials. The large-scale application of advanced packaging and new materials is still limited by process adaptation issues, and the limits of conventional silicon-based processes have not been fully lifted.

In the future, chip technology will continue to develop towards heterogeneous integration, ultra-low power consumption, AI-assisted design, and other directions. This article combines the technical ideas outlined in industry practice to provide practical reference for domestic chip design enterprises, promote the steady progress of the indigenous development of intelligent terminal chips, and better meet the practical needs of multi-scenario applications of intelligent electronic devices.

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