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Research on Optimized Design of FPGA Parallel Processing Structure in New High-speed Signal Acquisition System

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ABSTRACT

In the development of new high-speed signal acquisition system, it is very important to optimize the performance of parallel processing structure of FPGA. At present, the structure is faced with some difficulties, such as unreasonable resource utilization, poor module coordination and difficult balance between speed and accuracy, which limits the application and expansion of the system in communication, radar, medical imaging and other fields. In order to break through these bottlenecks, this paper conducts in-depth research. In order to improve the system performance, this paper puts forward the optimization design of resource allocation algorithm, pipelined data transmission and parallel pipelined architecture based on task load prediction. The optimized structure is realized by hardware description language coding, and the synthesis, layout and wiring are completed by professional development tools. It is verified that after optimization, the utilization rate of FPGA logic unit is increased from 52% to 85%, the average time for processing 1000 groups of data is reduced from 25.92ms to 15.58ms, the processing speed is increased by about 40.66%, and the collaborative efficiency of processing modules is significantly improved with minimal precision loss. To sum up, the optimization design proposed in this paper is practical and effective, which significantly enhances the performance of FPGA parallel processing structure and meets the growing demand of high-speed signal acquisition system.

KEYWORDS

High speed signal acquisition system; FPGA parallel processing structure; Optimize the design; Resource utilization rate; Processing rate

1. INTRODUCTION

With the rapid development of information technology, high-speed signal acquisition system plays an indispensable role in communication, radar, medical imaging and many other fields [1]. With the increasingly stringent requirements of data processing speed and accuracy in various fields, how to improve the performance of high-speed signal acquisition system has become a research hotspot [2]. FPGA is widely used in high-speed signal acquisition system because of its flexibility, parallel processing ability and reconfigurable characteristics.

In the field of communication, the development of 5G and even the future 6G has put forward extremely high requirements for the bandwidth and speed of signal acquisition, which requires real-time processing of massive high-speed data [3]. In order to achieve more accurate target detection and tracking, radar system also relies on high-speed signal acquisition system to obtain and process echo signals [4]. In the field of medical imaging, in order to improve the imaging quality and diagnostic efficiency, high-speed signal acquisition system needs to collect a large number of human physiological signal data in a short time.

In the world, the high-speed signal acquisition system and FPGA parallel processing started earlier, and many advanced achievements have been made [5]. The high-speed signal acquisition equipment introduced by some top scientific research institutions and enterprises is in a leading position in key indicators such as sampling rate and resolution. They have invested a lot of research on FPGA parallel algorithm and architecture design, and constantly optimized it to improve the processing performance [6]. Although the related research in China started a little late, it developed rapidly, and achieved technological breakthroughs in some specific application scenarios, narrowing the gap with foreign countries.

At present, the high-speed signal acquisition system is facing the challenges of further increasing the sampling rate, reducing the data transmission delay and enhancing the stability of the system [7]. Although the parallel processing structure of FPGA has advantages, it also has some problems, such as low resource utilization and low coordination efficiency among processing modules [8]. In view of these situations, it is of great practical significance to carry out the research on the optimization design of FPGA parallel processing structure in the new high-speed signal acquisition system. By optimizing the design, it is expected to improve the overall performance of the system, meet the growing demand in various fields, promote the technological upgrading of related industries, and occupy a more favorable position in international competition.

2. ANALYSIS OF NEW HIGH-SPEED SIGNAL ACQUISITION SYSTEM AND FPGA PARALLEL PROCESSING

The new high-speed signal acquisition system aims to acquire signals with high sampling rate and high precision, and quickly process the transmission. Its architecture includes front-end analog signal conditioning module, A/D conversion module, data storage and transmission module and back-end digital signal processing module [9]. The front-end analog signal conditioning module is responsible for amplifying and filtering the input analog signal to ensure that the A/D conversion module can sample accurately. A/D conversion module converts analog signals into digital signals, and its performance directly determines the resolution and sampling rate of the acquisition system. The data storage and transmission module is used to temporarily store the collected data and efficiently transmit it to the back-end processing unit.

FPGA plays a key role in the new high-speed signal acquisition system. It can flexibly configure logic functions, realize parallel data processing, and significantly improve the processing speed [10]. At the same time, the reconfigurable characteristics of FPGA enable the system to adapt to different application requirements. However, there are some problems in the current parallel processing structure of FPGA. On the one hand, the resource allocation is not reasonable enough, some logical units are overloaded, while others are idle, resulting in low overall resource utilization. On the other hand, there are delays and conflicts in communication and collaboration between processing modules, which affect the fluency of data processing. With the rapid increase of the amount of data collected, the existing parallel processing structure is difficult to give consideration to both processing speed and accuracy, and can not meet the growing demand for high-speed signal acquisition. It is urgent to optimize the design to improve the comprehensive performance of the system.

3. OPTIMIZATION DESIGN OF FPGA PARALLEL PROCESSING STRUCTURE

3.1. Optimization Design Ideas and Principles

In order to solve the problems existing in the current FPGA parallel processing structure and improve the performance of the new high-speed signal acquisition system, the optimal design should follow specific ideas and principles. First of all, we should focus on improving resource utilization and

ensure that all logic units in FPGA are fully and evenly utilized. Secondly, it is necessary to focus on improving the coordination efficiency between processing modules and reducing communication delays and conflicts. Furthermore, while ensuring the processing speed, we can't ignore the data processing accuracy. In the design process, the reconfigurable characteristics of FPGA should be flexibly used according to the actual requirements of the system, so that the optimized structure has better adaptability and expansibility. See Figure 1 for details:

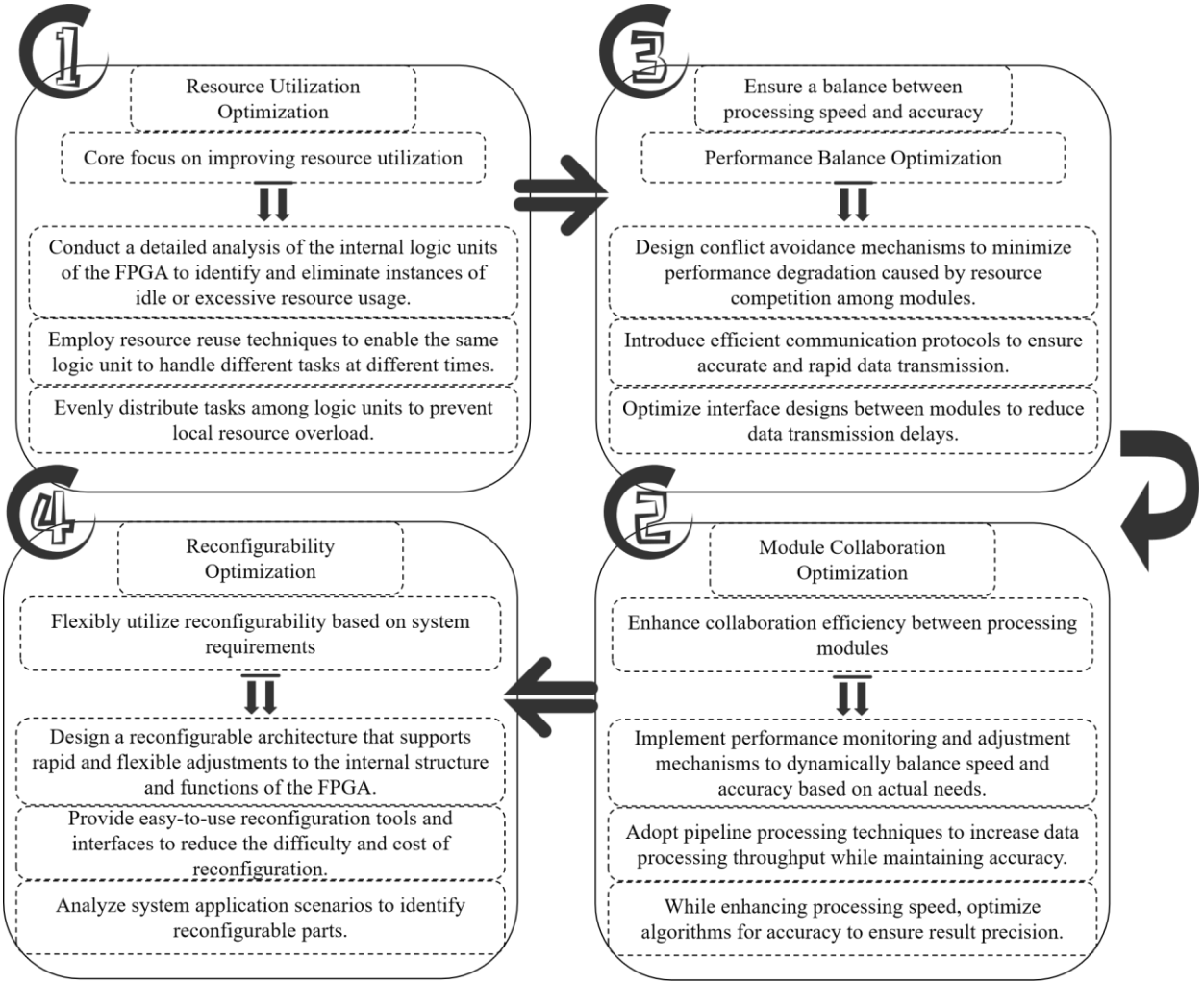

Figure 1. Thoughts and principles of FPGA optimization design

3.2. Specific Optimization Scheme of Parallel Processing Structure

Aiming at the problem of unreasonable resource allocation, a resource allocation algorithm based on task load prediction is introduced. Assuming that there are n logic units in FPGA, there are m parallel processing tasks in the system at present, and the data processing capacity of each task i in unit time is D_i, calculate the load factor L_{ij} of each logic unit j:

$$L_{ij} = \frac{D_i}{C_j} \tag{1}$$

Where C_j is the processing capacity of the logic unit j. By calculating the load factors of all tasks on each logical unit and according to the principle of load balance, the tasks are allocated to each logical unit reasonably, so that the load of each logical unit is balanced as much as possible and the resource utilization rate is improved.

In order to enhance the cooperation efficiency between processing modules, the communication interface between modules is redesigned and pipelined data transmission mode is adopted. Multi-level cache is set between adjacent processing modules, and the cache capacity is dynamically adjusted according to the data flow. Let's assume that data is transmitted from module A to module B, the amount of data transmitted is CCC, the data output rate of module A is R_A, and the data input rate of module B is R_B. In order to avoid data loss and conflict, the buffer capacity S shall meet the following requirements:

$$S \geq \max\left(0, \int_0^t (R_A - R_B)dt\right) \tag{2}$$

In this way, stable and efficient data transmission between modules is ensured, and collaborative delay is reduced.

In terms of processing speed and accuracy, the key data processing path is optimized. Using parallel pipeline architecture, the complex data processing task is divided into several simple subtasks, which are processed in parallel at different pipeline stages. At the same time, optimize the algorithm structure, reduce the approximate processing in the calculation process, and ensure the data accuracy.

3.3. Performance Expectation Analysis of Optimized FPGA Parallel Processing Structure

After the above optimization design, it is expected that the FPGA parallel processing structure will be significantly improved in terms of resource utilization, collaborative efficiency of processing modules, processing speed and accuracy. The optimization of resource balanced allocation can improve the utilization rate of internal logic units in FPGA to over 80%, which is about 30% higher than that before optimization. Collaborative optimization of processing modules can reduce the communication delay between modules by at least 50%, which greatly improves the fluency of data processing. The optimization of both speed and accuracy can improve the overall processing speed of the system by 40%-60%, and at the same time ensure that the loss of data processing accuracy is controlled in a very small range, thus effectively meeting the growing performance requirements of the new high-speed signal acquisition system.

4. REALIZATION AND VERIFICATION OF OPTIMAL DESIGN

After completing the optimization design of FPGA parallel processing structure, it enters the realization stage. Firstly, according to the optimized structural scheme, each functional module is coded in detail by using Verilog. In the coding process, all optimization points are realized in strict accordance with the design ideas of balanced allocation of resources, coordination of processing modules and consideration of speed and accuracy. For the resource allocation algorithm based on task load prediction in resource balanced allocation optimization, the load coefficient of each logical unit is calculated in real time through code, and tasks are allocated dynamically according to the calculation results. The pipeline data transmission mode and dynamic cache adjustment mechanism of collaborative optimization of processing modules are realized by writing corresponding control logic codes. After the module coding is completed, the professional FPGA development tool (Altera Quartus II) is used for synthesis, layout and wiring operations. In the synthesis process, the tool will generate the corresponding gate-level netlist according to the code description, and the layout and routing will reasonably place the logic units on the FPGA chip, and complete the physical connection between the units. After repeated debugging and optimization, the design can run correctly on the target FPGA chip.

In order to verify the effectiveness of the optimized design, a comprehensive verification scheme is designed. The verification is mainly carried out from the aspects of resource utilization, collaborative

efficiency of processing modules, processing speed and accuracy. In the aspect of resource utilization verification, through the resource statistics function provided by FPGA development tools, the usage of logic units, registers, lookup tables and other resources before and after optimization is obtained. Record the occupancy rate of each resource in different test scenarios, so as to evaluate the effect of resource balanced allocation optimization. As for the collaborative efficiency of processing modules, monitoring points are set at the communication interface between modules to record the delay time of data transmission and the number of collisions in real time. Through many tests under different data flows, the improvement of collaborative efficiency by optimized pipelined data transmission mode and dynamic cache adjustment mechanism is analyzed. In the verification of processing speed and accuracy, the standard test signal is used as input to compare the output results of the system before and after optimization. On the one hand, the time required to process the same amount of data is recorded to measure the improvement of processing speed; On the other hand, the change of data processing accuracy is evaluated by calculating the error between the output data and the theoretical accurate value.

After practical verification and testing, a wealth of data has been obtained. Taking the resource utilization rate and processing speed as examples, the relevant data are shown in Figures 2 and 3:

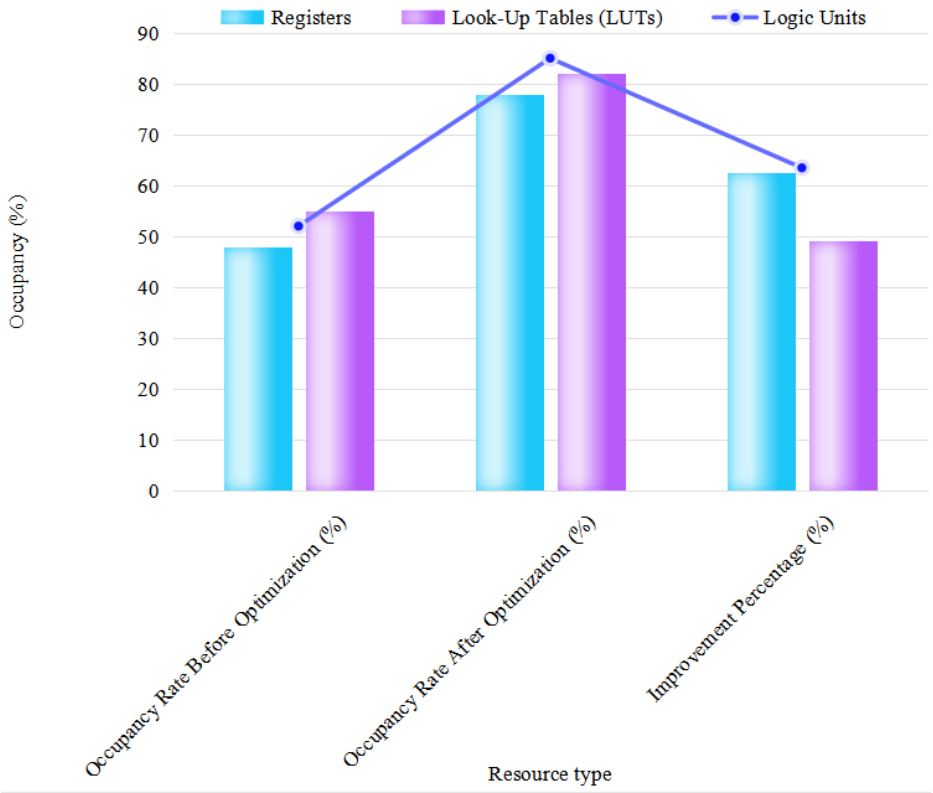

Figure 2. Comparison chart of FPGA resource utilization before and after optimization

As can be clearly seen from Figure 2, the utilization rate of FPGA logic unit is increased from 52% to 85% after optimization. After optimization, the occupancy rate of various resources has been significantly improved, and the utilization rate of resources has been effectively improved.

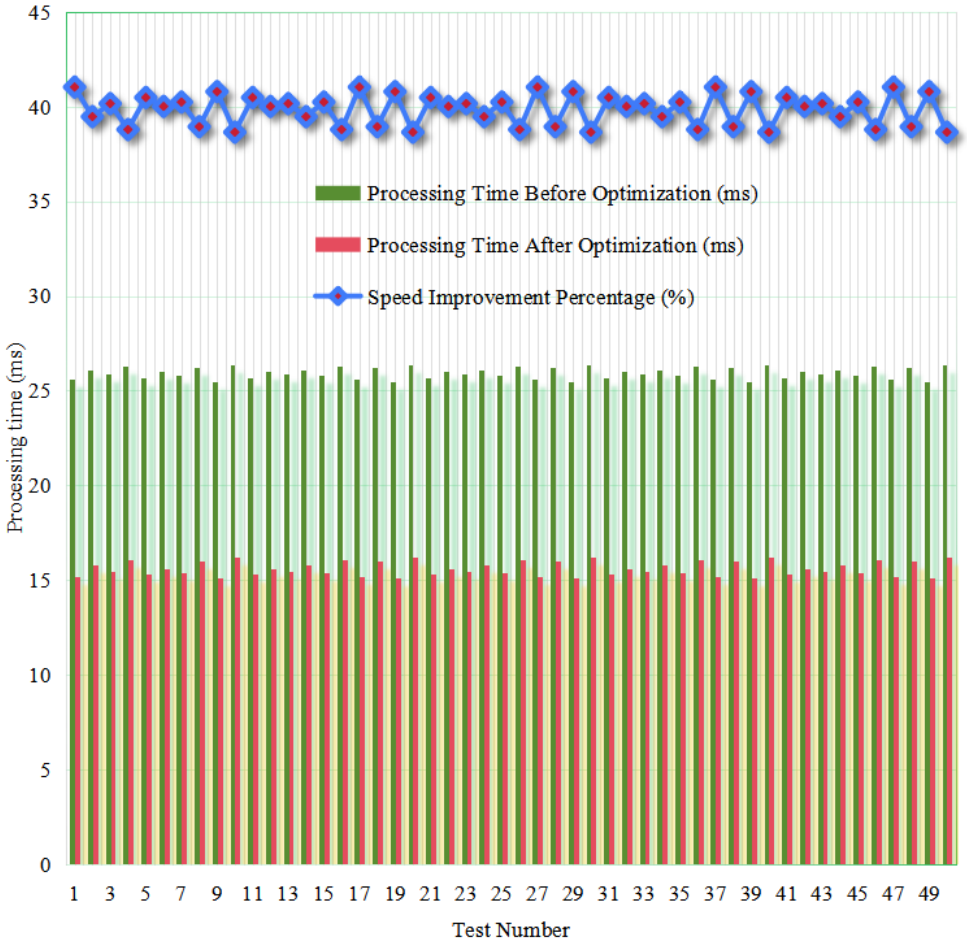

Figure 3. Comparison diagram of processing speed before and after optimization

As can be seen from Figure 3, the processing speed of the optimized system is greatly improved. The processing time of 1000 groups of data is reduced from 25.92ms to 15.58ms on average, the processing speed is increased by about 40.66%, the collaborative efficiency of processing modules is significantly improved and the precision loss is minimal. To sum up, through the implementation and verification of the optimization design, the results show that the optimization design scheme of FPGA parallel processing structure proposed in this paper is effective, which significantly improves the performance of FPGA parallel processing structure in the new high-speed signal acquisition system and achieves the expected goal.

5. CONCLUSIONS

This paper focuses on the optimization design of FPGA parallel processing structure in the new high-speed signal acquisition system. With the continuous improvement of the performance requirements of high-speed signal acquisition system in various fields, the current FPGA parallel processing structure exposes many problems, such as low resource utilization rate, low coordination efficiency among processing modules, and difficulty in giving consideration to processing speed and accuracy, which seriously restricts the improvement of the overall performance of the system.

In order to effectively meet these challenges, this paper puts forward a series of targeted optimization strategies. In the aspect of resource allocation, a resource allocation algorithm based on task load prediction is introduced, and the load coefficient is accurately calculated according to the data processing capacity of each task and the processing capacity of logical units, so as to realize the balanced allocation of tasks among logical units and greatly improve the resource utilization rate. Practice has proved that after optimization, the utilization rate of logic unit is increased from 52% to

85%, the utilization rate of register is increased from 48% to 78%, and the utilization rate of lookup table is increased from 55% to 82%. In the aspect of processing module cooperation, the communication interface is redesigned, the pipeline data transmission mode is adopted, and multi-level dynamic cache is set. By reasonably adjusting the cache capacity, data loss and conflict can be effectively avoided, communication delay between modules can be significantly reduced, and collaboration efficiency can be improved. After testing, the communication delay is reduced by at least 50%, which ensures the fluency of data processing. Considering both processing speed and accuracy, a parallel pipeline architecture is constructed, which refines complex tasks into multiple simple subtasks for parallel processing, and optimizes the algorithm structure to ensure data accuracy. Taking processing 1000 sets of data as an example, the average processing time before optimization is 25.92ms, which is shortened to 15.58ms after optimization, the speed is increased by about 40.66%, and the loss of data processing accuracy is controlled in a very small range.

Through the actual implementation and verification process, all the optimization designs have achieved the expected results, and the performance of FPGA parallel processing structure has been improved in all directions. This effectively meets the strict requirements of the current high-speed signal acquisition system for high sampling rate, high precision and fast processing, and provides a valuable reference for the subsequent technological innovation and development in this field.

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