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SMG-YOLO: PCB Defect Detection Algorithm Based on Improved Multiscale Fusion Optimization with YOLOv11n

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ABSTRACT

Printed Circuit Board (PCB) is the substrate of electronic parts, the demand is great, carrying the layout of the circuit components and wires, and its good or bad on the quality of electronic products has important impact! To address the limitations of insufficient detection accuracy and suboptimal real-time performance in current PCB surface defect detection methodologies, this study proposes SMG-YOLO, an enhanced YOLOv11n architecture. The proposed framework integrates three principal innovations: 1) a multi-scale fusion convolution module (MSCB) synergistically combined with C3k2 blocks to optimize feature extraction across spatial resolutions; 2) replacement of the conventional Neck structure with a hierarchical SlimNeck architecture to enhance computational efficiency; and 3) implementation of a Global Context Aggregation mechanism to refine defect localization precision. Experimental validation demonstrates that SMG-YOLO achieves state-of-the-art performance metrics, including a mean average precision (mAP50) of 95.5% and a recall rate of 97.0%, surpassing the baseline YOLOv11 model by 4.3% and 2.0%, respectively. Furthermore, the optimized architecture attains a Computational amount of only 7.7 GFLOPs and a processing speed of 232.8 FPS, satisfying stringent industrial requirements for high-throughput inspection.

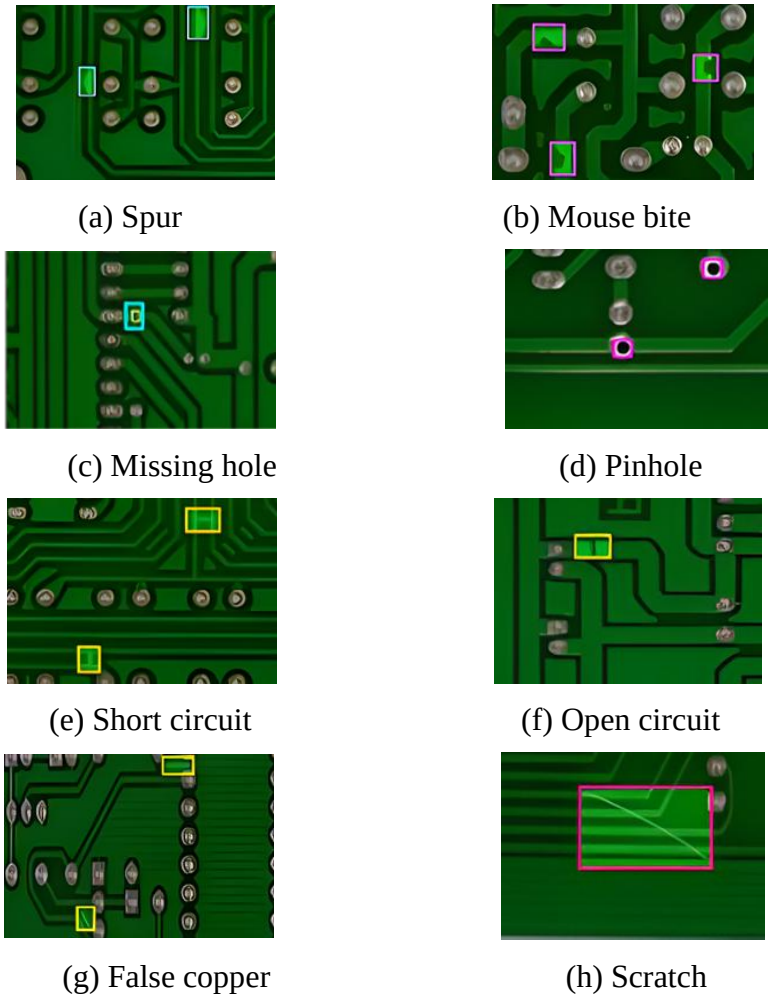
KEYWORDS

Printed circuit board (PCB); Defect detection; Deep learning; YOLOv11

1. INTRODUCTION

The rapid advancements in 5G communications, Internet of Things (IoT), and new energy vehicle technologies have driven substantial growth in printed circuit board (PCB) demand across emerging technological sectors. This surge has precipitated a corresponding evolution in PCB manufacturing methodologies toward achieving superior performance metrics, elevated density parameters, and intricate complexity benchmarks [1]. However, the fabrication of PCBs inherently involves multistage protocols comprising photolithography, etching, lamination, and drilling operations, each stage introducing potential failure modes. These manufacturing processes remain vulnerable to environmental variability (e.g., temperature/humidity fluctuations) and operator-induced variances, consequently predisposing finished boards to critical defects [2]. These latent defects can induce structural integrity compromises (e.g., conductive path discontinuity) and functional impairments (e.g., impedance mismatch), progressively degrading the operational reliability of electronic systems while compromising energy efficiency metrics. This operational imperative establishes PCB defect detection as a critical quality assurance requirement, serving as a technical safeguard to mitigate non-conformance costs, prevent post-deployment field failures, and optimize material utilization

efficiency [3]. PCB defects are systematically classified into two primary categories: surface-layer anomalies and solder joint imperfections. This study specifically targets surface defect detection due to its critical impact on signal transmission fidelity. Predominant surface defects include Missing hole, Mouse bite, Open circuit and Short circuit et al, To ensure manufacturing quality assurance and enhance defect taxonomy comprehensiveness, eight representative surface defect variants were rigorously selected as the investigation subjects, with detailed morphological characteristics illustrated in Fig. 1 (a-h).



(a) Spur (b) Mouse bite

(c) Missing hole (d) Pinhole

(e) Short circuit (f) Open circuit

(g) False copper (h) Scratch

Figure 1. Types of defects

During initial industrial implementation phases, PCB surface defect detection predominantly relied on human visual assessment and electrical continuity testing via probe arrays [4]. Traditional methods for PCB surface defect detection have obvious limitations in practical applications and are gradually being eliminated due to cost, detection efficiency and accuracy. The evolution of PCB defect detection methodologies has undergone substantial refinement in recent years, with automated optical inspection (AOI [5]) systems progressively establishing themselves as integral components of modern manufacturing workflows. AOI This non-destructive inspection system integrates machine learning-enhanced image processing with high-fidelity optical sensing for automated characterization of PCB surface defects.

Within the evolutionary trajectory of computational intelligence paradigms, seminal machine learning architectures including Support Vector Machines (SVM) [6], Artificial Neural Networks (ANN) [7], Genetic Algorithms (GA) [8], and Decision Tree (DT) [9]. classifiers have been systematically implemented in PCB defect diagnostics framework. The ascendancy of deep learning-based object detection has established computational superiority over conventional machine learning approaches, demonstrating enhanced precision and real-time processing capabilities in industrial

visual inspection [10]. Kewen et al [11] devised a GCC-YOLO architecture integrating global attention mechanisms with ConvMixer [12]-optimized prediction heads and BiFPN [13]-based multi-scale feature fusion, achieving 5.7% parameter reduction versus baseline YOLO models while sustaining 89.2% mAP accuracy at 42 FPS inference speeds. Xiao et al [14] engineered CDI-YOLO through synergistic integration of coordinate attention (CA) [15] modules and depthwise separable convolutions (DSConv) [16], augmented by an Inner-CloU loss function within YOLOv7-tiny [17] frameworks, attaining 93.1% detection accuracy with 34% latency reduction over conventional implementations. Mo et al [18]. innovated a YOLOv5 [19] variant featuring SE-ENV2 [20] backbone networks, GC-Neck hierarchical feature extractors, and TSCODE [21] detection headers, achieving 96.4% precision with 41% fewer computational operations than standard configurations. These advancements collectively validate neural architecture search (NAS)-optimized CNNs as the prevailing methodology for PCB inspection, balancing sub-100ms inference latency, micron-level defect resolution, and hardware-constrained deploy ability.

Advancing deep learning detection techniques impose escalating demands on PCB defect inspection systems regarding accuracy, processing speed, and model efficiency. Current architectures face inherent limitations in detecting sub-millimeter defects that occupy minimal image areas, fundamentally constraining multi-scale feature extraction capabilities and resulting in incomplete defect characterization. To resolve these challenges, we propose SMG-YOLO—an optimized YOLOv11 [22] variant integrating three core enhancements: SlimNeck for parameter-efficient feature fusion ,C3k2-MSCB module enabling multi-dimensional defect feature capture, GAM attention mechanism strengthening critical defect saliency. This synergistic redesign systematically improves micro-defect detection capacity while preserving real-time inference capabilities and model compactness.

2. METHODOLOGY

2.1. SMG-YOLO Network Infrastructure

The proposed SMG-YOLO architecture (Fig. 2) introduces three strategic enhancements to optimize PCB defect detection:

(1) Slim-Neck Optimization: Replaces the standard neck with a lightweight structure employing GSConv and VoV-GSCSP modules, enhancing multi-scale feature fusion efficiency while reducing computational redundancy for micro-defect characterization

(2) Multi-Scale Convolution Block (MSCB): Integrated with C3k2 to enable hierarchical feature extraction across convolutional layers, balancing multi-receptive-field analysis with computational efficiency for diverse defect patterns

(3) Global Attention Mechanism (GAM): Implements dual-dimensional attention (channel-spatial) to amplify defect-related features while maintaining parameter efficiency.

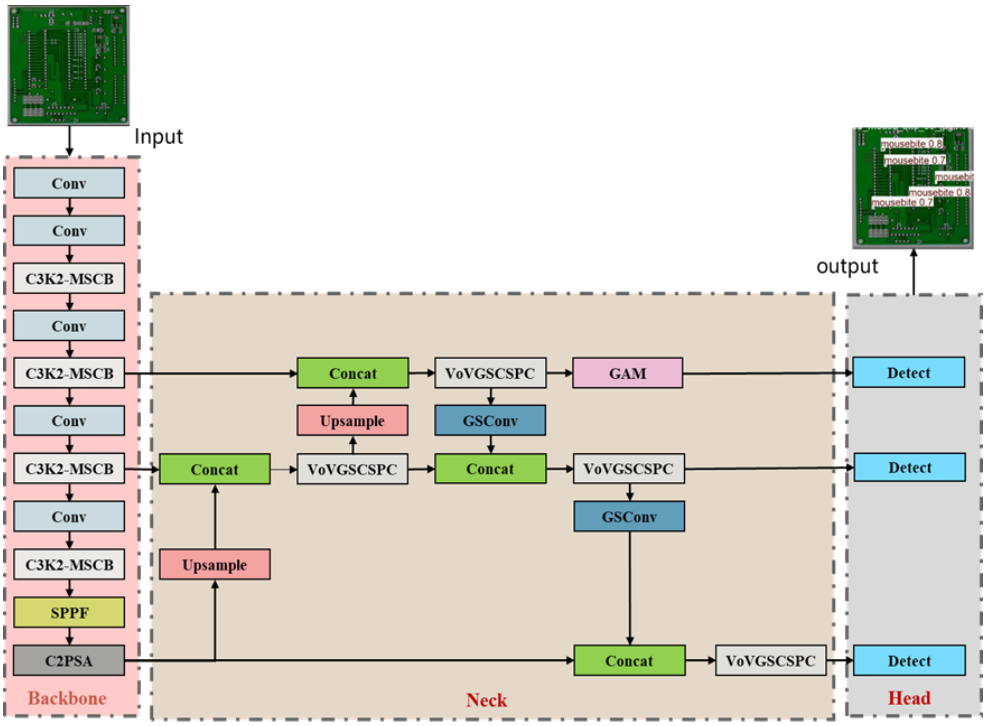


Figure 2. SMG-YOLO network structure

2.1.1. Slim-Neck

Hulin Li et al [23]. developed a lightweight Slim-Neck architecture to maintain detection accuracy on resource-constrained devices. This design combines GSConv lightweight convolution with VoV-GSCSP's efficient cross-stage feature fusion, optimizing computational efficiency while preserving detection precision. For PCB defect inspection, Slim-Neck reduces model complexity and enhances feature processing effectiveness for micro-defects compared to conventional neck structures.

(1) GSConv

Whereas time complexity is usually defined by floating point computations (FLOPs), the following equations represent the time complexity of SC(1) , DSC(2) and GSConv(3):

$$SC: O(W \cdot H \cdot K_1 \cdot K_2 \cdot C_1 \cdot C_2) \tag{1}$$

$$DSC: O(W \cdot H \cdot K_1 \cdot K_2 \cdot C_1) \tag{2}$$

$$GSConv: \frac{O([W \cdot H \cdot K_1 \cdot K_2 \cdot C_2]}{2 \cdot (C_1 + 1)} \tag{3}$$

The convolutional layer parameters are defined as follows: W × H: Dimensions of the output feature map (width × height), $K_1 \times K_2$: Convolution kernel dimensions, C_1: Input feature map channel depth (equivalent to per-kernel input channels), C_2: Output feature map channel depth.

(2) VoV-GSCSP

The GS-bottleneck module is first introduced in VoV-GSCSP, followed by an efficient cross-stage (CSP) network module designed using the One-Shot [24] strategy. The GS-bottleneck module fuses the SC-processed features with the image features from the two GSConv treatments, realizing the same model-learning capability as SC and reduces the computational effort by about 50%, and the

cross-stage network (CSP) improves the computational accuracy and reduces the inference time by aggregating them.

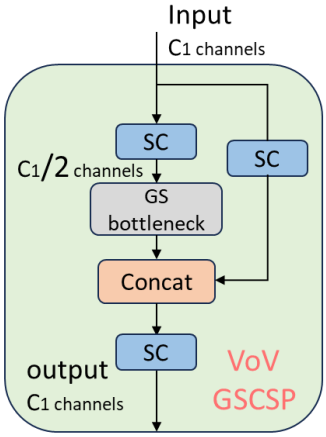


Figure 3. GS-bottleneck structure

2.1.2. C3k2-MSCB

Mustafa et al [25]. scholars proposed a new efficient multi-scale convolutional decoder EMCAD in their study of medical image segmentation, of which the MSCB module is used in this paper. The MSCB module performs convolutional operations at multiple scales in order to capture image features of different layers while maintaining the computational efficiency of depth-divisible convolution and assisting with feature extraction capability and feature fusion capability. In this case, the MSDC module performs convolutional operations on the input feature maps with multi-scale convolutional kernels separately, and operates on the convolutional kernels by means of depth-divisible convolution, and finally fuses (joins or sums) the features at different scales. In this paper, after fusion with C3k2 module, it can assist YOLOv11 to perform more efficient feature extraction and fusion capability for PCB defect images.

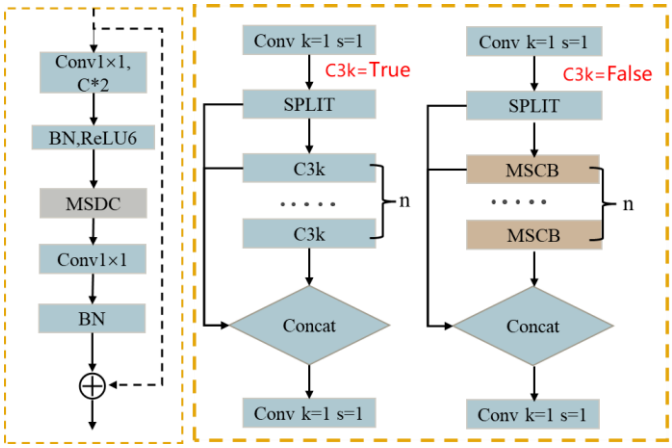


Figure 4. MSCB and C3k2-MSCB

2.2. GAM Attention Mechanism

Helmholtz et al [26] designed a Global Attention Mechanism (GAM) to enhance neural network performance for diverse computer vision tasks by mitigating information loss and amplifying global interactions. the GAM retains the spatial attention module from CBAM [27] while redesigning its submodules. The MLP initially compresses the channel dimension via a bottleneck layer (reduction factor r), followed by feature expansion to restore the original dimensionality. Finally, the channel

attention coefficients MC(F1) are generated through Sigmoid activation, with their mathematical derivation formalized in Equation (5).

$$F_2 = M_C(F_1) \otimes F_1 \tag{4}$$

$$M_C(F_1) \otimes F_1 = sigmoid[K_1 \cdot \mathrm{Re}\,LU(w_2(w_1 K_1^T + b_1) + b_2)$$

The attention maps first undergo dual 7×7 convolutions for spatial fusion, with channel compression via reduction ratio r, while eliminating pooling layers to preserve feature integrity. Following channel attention protocol, spatial coefficients MS(F2) are activated by Sigmoid. Final output F3is obtained through element-wise multiplication of attention maps, with full derivation in Equation (6).

$$F_3 = M_S(F_2) \otimes F_2 \tag{5}$$

$$M_S(F_2) \otimes F_2 = sigmoid[ConvBN(ConvBNRELU(K_2))]$$

3. EXPERIMENTATION AND ANALYSIS

To validate SMG-YOLO's efficacy in PCB defect detection and module enhancements, we conducted comparative experiments on datasets: *TEST-PCB* (self-collected). The model was benchmarked against contemporary detectors (YOLOv11s, YOLOv8n/s, YOLOv5n/s) across standard metrics. Ablation studies through sequential module removal/replacement in the enhanced network were performed to verify architectural necessity, with quantitative comparisons against the full SMG-YOLO configuration.

3.1. Experimental Environment

The computational environment utilized PyTorch 2.1.0 with CUDA 11.8 acceleration on Python 3.9.1, running Windows 10 OS. Hardware specifications included an Intel Core i5-12490F CPU, 16GB RAM, and an NVIDIA, GeForce RTX 3060Ti GPU (8GB VRAM). Training configurations employed:300 training epochs with batch size 16, SGD optimizer (initial learning rate: 0.01, momentum: 0.937), Mixed-precision training implementation.

3.2. Experiment Dataset

The TEST-PCB dataset was curated through systematic collection of high-definition PCB defect images from public repositories, focusing on eight critical surface defects: False copper(a), Missing holes(b), Mouse bites(c),Open circuits(d), Pinhole(e), Scratch(f), Short circuits(g) and Spur(h) (3,134 raw samples). Using Roboflow annotation platform, we implemented multi-strategy augmentation (rotation, cropping, noise injection, brightness variation) to enhance model robustness and environmental adaptability, expanding the dataset to 6,256 images. Final data partitioning followed an 8:1:1 ratio for training/validation/testing sets. Defect category distributions are quantified in Figure 5.

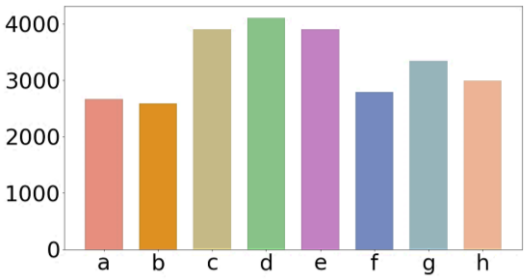


Figure 5. TEST-PCB data set

3.3. Evaluation Metrics

In this study, mean average precision (mAP), average precision (AP), FPS, Recall, and FLOPs (floating point operations) were used as metrics to evaluate model performance. The precision P and recall R ,AP, FPS for a single category are calculated as shown in Equation (6)~(8).

$$P = \frac{T_P}{T_P + F_P} \times 100\%, R = \frac{T_P}{T_P + F_N} \times 100\% \tag{6}$$

$$AP = \int_0^1 P(R)dR, mAP50 = \frac{\sum_{i=1}^{N} AP_i}{N} \tag{7}$$

$$FPS = \frac{F_N}{T} \tag{8}$$

3.4. Ablation Experiments

To assess the beneficial impacts of integrating the Slim-Neck architecture, C3k2-MSCB modules, and GAM attention mechanism on PCB defect detection, three model variants were developed based on YOLOv11n: S-YOLO (Slim-Neck), SM-YOLO (S-YOLO + C3k2-MSCB), and SMG-YOLO (SM-YOLO + GAM). Ablation studies conducted on the TEST-PCB dataset (Table 1) confirm the efficacy of these improvements. The C3k2-MSCB module, through multi-scale convolutional operations, significantly enhances detection accuracy by capturing hierarchical features critical for small-defect identification, yielding a 2.3% mAP50 increase, 91.4% precision, and 2.2% F1-score/1% recall gains over the baseline while preserving computational efficiency.

Despite minor inference speed tradeoffs, Slim-Neck and GAM further optimize performance: Slim-Neck improves feature fusion efficiency, while GAM mitigates global information loss. Full integration (SMG-YOLO) achieves 92% F1-score and 97% recall, demonstrating the complementary nature of these modules. The progressive mAP50 improvement across variants validates their compatibility, with Slim-Neck and GAM enhancing processing accuracy without substantially affecting model size or speed. This balanced architecture proves effective for industrial-scale PCB inspection tasks.

Table 1. Results of ablation experiments

S	M	G	Precision(%)	Recall(%)	F1(%)	mAP@0.5(%)	GFLOPs/109	FPS
			85.0	95.0	88.8	91.2	6.3	275.7
√			90.1	96.0	90.0	93.2	6.3	240.7
	√		91.4	96.0	91.0	93.5	6.2	256.6
		√	87.6	96.0	90.0	93.0	7.8	241.3
√	√		89.9	97.0	92.0	94.6	6.2	244.7
	√	√	87.3	97.0	92.0	94.7	7.8	205.0
√		√	86.6	97.0	92.0	95.1	7.8	232.1
√	√	√	91.7	97.0	92.0	95.5	7.7	232.8

Collectively, these enhancements enable the final SMG-YOLO model to achieve 4.3% higher overall accuracy, 2% improved recall, 6.7% precision gain, and 92.0% F1-score compared to the baseline YOLOv11n, while maintaining a compact model size and real-time computational efficiency that fulfills industrial inspection demands. The ablation experiments conclusively validate that the proposed improvements to the YOLOv11n framework enhance PCB surface defect detection precision without compromising practical deployment performance, thereby balancing technical advancement with engineering applicability.

3.5. Comparative Experiments

On the TEST-PCB dataset, SMG-YOLO was rigorously compared with five leading object detection models—YOLOv11s, YOLOv8s, YOLOv5s, YOLOv8n, and YOLOv5n—under identical experimental settings, using AP, mAP50, GFLOPs, and FPS as evaluation metrics. Results are summarized in Table 2.

Table 2. Comparative experimental results

Method	mAP/%	GFLOPs/109	FPS
YOLOv5n	91.2	5.8	291.4
YOLOv5s	93.4	18.8	186.9
YOLOv8n	92.4	6.8	286.4
YOLOv8s	94.5	23.4	177.3
YOLOv11n	91.2	6.3	275.7
YOLOv11s	96.8	27.0	154.7
SMG-YOLO	95.5	7.7	232.8

As evidenced in Table 2, the proposed SMG-YOLO demonstrates superior overall performance in PCB defect detection. While its mAP50 slightly trails YOLOv11s, it outperforms all other networks in this metric. Compared to "s-series"models- YOLOvs(5\8\11), SMG-YOLO achieves 60 FPS speed advantage and 67% lower computational load (GFLOPs) with comparable accuracy—for instance, maintaining 1% higher mAP50 than YOLOv8s despite requiring only one-third of its computational cost. Notably, SMG-YOLO maintains competitive GFLOPs and FPS metrics relative to "n-series" counterparts YOLOv5n, YOLOv8n, YOLOv11n. In defect-specific evaluations, SMG-YOLO significantly improves detection accuracy for historically challenging categories: Missing Hole (79.3% → 96.8%, +17.5%) and Short Circuit (84.6% → 94.1%, +9.5%) compared to the YOLOv11n baseline.

Figure 6 illustrates the training trajectory: SMG-YOLO's mAP50 growth rate initially parallels YOLOv11n but surpasses it after 50 epochs. Although SMG-YOLO's progression slows temporarily at epoch 100, it resumes accelerated growth post-epoch 150, while YOLOv11n's curve plateaus due to overfitting.

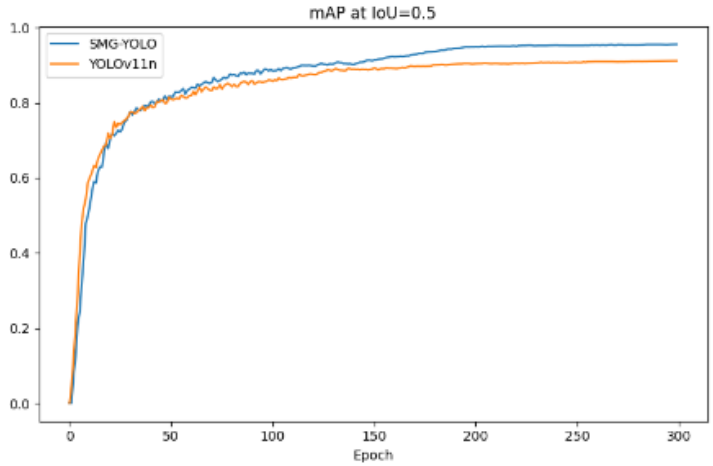


Figure 6. Change in mAP values before and after improvement

Comprehensively compared with the current mainstream algorithms SMG-YOLO's mAP50 value reaches a satisfactory 95.5%, but also has a smaller amount of computation and up to 232.8FPS computation speed, showing excellent general-purpose performance.

4. CONCLUSIONS

This study addresses the limitations of YOLOv11 in PCB surface defect detection by proposing SMG-YOLO, an enhanced architecture integrating SlimNeck for efficient feature fusion, C3k2-MSCB for multi-scale feature extraction, and a Global Attention Mechanism (GAM) to prioritize defect-related spatial-channel interactions. These innovations collectively achieve superior accuracy and computational efficiency.

Experimental validation on TEST-PCB demonstrates SMG-YOLO’s advancements: 95.5% mAP50 respectively, representing 4.3% improvements over YOLOv11n. The model also elevates F1-score, recall, and precision by 3.1–5.2% while maintaining near-baseline computational efficiency (+1.4 GFLOPs) and real-time speeds (232.8–240.3 FPS).

SMG-YOLO outperforms conventional methods in both speed and accuracy, offering practical value for industrial PCB inspection systems. Future work will focus on enhancing defect localization precision and mitigating background interference through advanced attention mechanisms. Further optimization via model compression and pruning will enable deployment on resource-constrained edge devices.

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