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High Wideband Digital Oscilloscope Design

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ABSTRACT

In most test applications, acquisition and analysis involving simultaneous processing of analog and digital signals. However, the bandwidth of most mainstream digital oscilloscopes is limited to 100 MHz, which is unable to meet the testing needs of high-frequency signals in complex electronic systems [1], and therefore, high-bandwidth digital oscilloscopes have emerged. Based on this background, this paper designs a digital oscilloscope hardware platform with high bandwidth by integrating FPGA and ARM technologies, aiming to meet the rigorous testing requirements of modern electronic systems. The FPGA module is based on the xc7s75fgga676 chip, which is mainly responsible for ADC control, data processing and frequency measurement functions. AM5708 is selected as the ARM module to realize the trigger, time base, amplitude and automatic setting functions of the oscilloscope. In order to ensure the accuracy and fidelity of waveform changes, the Sinc function interpolation method is used. This design further improves the acquisition bandwidth and processing speed on the basis of traditional MSO (Mixed Signal Oscilloscope) oscilloscopes, which is of great significance for the acquisition and processing of high-speed signals.

KEYWORDS

Equally spaced draw points; FIFO storage; Sinc interpolation

1. INTRODUCTION

With advances in microelectronics and digital signal processing (DSP) technology, digital oscilloscopes are able to process complex signals more efficiently and provide higher performance [1-2]. The increasing complexity of modern electronic devices and systems requires higher-level test and measurement tools to ensure their performance and reliability. Currently, most of the mainstream digital oscilloscopes are limited to a bandwidth of 100MHz, which is not able to do specific analysis of signals above 100MHz [3].

This paper proposes a high-bandwidth digital oscilloscope, the device can pick up the highest input bandwidth of 200MHz signals, the sampling rate of 1GSPS, in addition to the design of an algorithm for automatic measurement of the amplitude and frequency of the signal under test, and time base, amplitude, automatically set up to the most suitable for the signal observation of the gear (the vertical direction of the waveform accounted for about 60% of the vertical direction of the waveform display area of the screen, signal), and the time base, amplitude, and time base are automatically set to the most suitable for the observation of the signal. Each cycle accounts for about 3-5 time base frames), and automatically set the trigger level to achieve a stable display of the signal, you can change the time base through the time base knob, change the amplitude through the amplitude knob, and can display this information on the screen.

2. OVERALL DESIGN

2.1. Overall Design Block Diagram

This design involves the use of multiple platforms, including FPGA and ARM, etc. In order to realize the various functions, it is necessary to design and implement each platform and ensure that they can work together smoothly. In addition, attention needs to be paid to the data interaction, communication and protocols between the various platforms to ensure the reliability and performance of the entire system. In terms of the design of the ARM side, it is necessary to realize the functions of channel amplitude and displacement control, data sampling and interpolation, signal calibration, waveform display, and so on. Channel amplitude and displacement control needs to control the output of the hardware circuit in real time according to the user's input; data sampling and interpolation needs to process the received data to improve the details and accuracy of the waveform; signal calibration needs to be able to accurately calibrate different signals; waveform display needs to display the data using the visualization interface, and the block diagram of the overall scheme is shown in Figure 1.

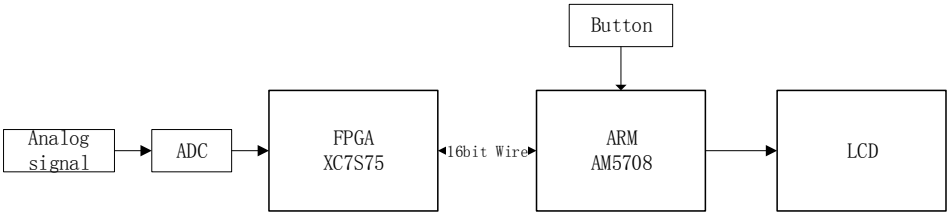

Figure 1. Overall design block diagram

2.2. ARM Design

This design firstly uses ARM to read the data from the FIFO of FPGA, after reading the data, the trigger is set on the data to stabilize the waveform after which the waveform is transformed by key control, finally, the waveform is smoothed and filtered, and refreshed and displayed on the LCD screen.

In terms of interface design, this oscilloscope uses a 700×400 pixel LCD screen, so the screen size needs to be considered. In order to realize a beautiful interface design, the interface is divided into three areas: upper, middle and lower. the three areas of the interface are: top parameter display area, waveform display area and bottom parameter display area.

2.2.1. Time base function design

For the design of the time base function, the variable time base scheme is adopted. Users can adjust the time base parameter by knob or key to change the period of the oscilloscope. The time base block setting interval of this intelligent oscilloscope is from 1ns/div to 500ms/div, with a total of 27 blocks, and the step value between these blocks is 1-2-5.

The system reads frequency data from the FIFO, including the high octet and low octet of the frequency. These two parts are spliced by shifting to get the complete frequency value. Next, the frequency interval is divided according to the frequency so that the time base can be automatically adjusted under different frequency intervals. For different frequency intervals, corresponding time base adjustment values are designed for the time base. In addition, the corresponding adjustment is made according to the left or right rotation of the knob, where the left rotation increases the time base adjustment value while the right rotation decreases it. The time base conversion is interpolated and the corresponding waveform is displayed.

In the choice of interpolation method for time base transformation, we use sin(x)/x function interpolation. This interpolation method is based on the Sinc function [4-5], which can theoretically achieve a distortion-free interpolation effect and better maintain the details and accuracy of the

waveform. sin(x)/x function interpolation has a high interpolation accuracy and waveform fidelity, and can accurately reconstruct the details of the original waveform. By utilizing the characteristics of the sinc function, it can effectively suppress the generation of aliasing and artifacts and provide more accurate and smooth waveform transformation results. Therefore, the sin(x)/x function interpolation is most suitable to meet the design requirements of the oscilloscope, which can effectively realize the time base transformation and maintain the high quality and accuracy of the waveform.

2.2.2. Amplitude Function Design

The frequency range of this oscilloscope is 1Hz~200MHz, due to the influence of high frequency signal amplitude attenuation, the oscilloscope needs to be able to adjust the amplitude of the waveform [6]. For this reason, the amplitude block interval of this oscilloscope is 1mv/div~10V/div, and a total of 13 blocks are designed, and their step values are 1-2-5.

By reading the maximum and minimum values of the waveform and calculating the difference between them, the amplitude peak-to-peak value is obtained, and then the actual value of the amplitude peak-to-peak value is calculated using the formula.

At the same time, it is also necessary to determine whether the Auto button is pressed or not. If the Auto button is pressed, the display of the waveform will be automatically adjusted according to the peak-to-peak amplitude value to ensure that the vertical direction occupies more than 60% of the display. Alternatively, adjustments can be made with the Magnitude Grid knob. By rotating the knob to the left or right, different values can be set to adjust the amplitude of the waveform. Finally, the adjusted waveform is output for display.

2.2.3. Trigger Function Design

Trigger function is one of the key functions in the oscilloscope, which is used to accurately capture and display the waveform of a specific event or signal [7]. The implementation of the trigger function in this oscilloscope design helps to observe and analyze a specific part of the signal effectively to meet the triggering needs of the project.

Upon entering the capture and trigger function, the trigger level is first calculated and the associated trigger variables are initialized. Then, the trigger point is found by traversing the array of data transferred in. If the trigger point is found, the waveform is drawn and the display is refreshed; if the trigger point is not found, the array continues to be traversed to find the trigger point.

2.2.4. Automatic Setup Function Design

The automatic setup function is a key difficulty in this oscilloscope design. Its purpose is to quickly configure the oscilloscope parameters to adapt to different signals and application scenarios. With the auto-setup function, the time required to manually adjust parameters can be reduced and complexity can be minimized, efficiency can be improved, and accurate measurement results can be obtained.

This oscilloscope is equipped with an auto setup function that automatically optimizes the oscilloscope settings according to the characteristics of the input signal. The function automatically recognizes parameters such as frequency, amplitude, and position of the signal and adjusts the oscilloscope's time base, amplitude, and position settings accordingly to ensure that the signal is clearly displayed and accurately measured.

The auto setup function is integrated in the key reading module. When the auto key is pressed, the system will adjust the frequency and peak-to-peak value of the signal accordingly [8]. By acquiring these adjustment parameters, the system can change the period and amplitude of the waveform, etc. to obtain the ideal waveform display. In auto setting mode, the waveform of each cycle occupies 3~5 time base frames and the vertical amplitude exceeds 60% of the total amplitude. If the Auto button is not pressed, the user can use the knob to adjust the amplitude, period and position of the waveform to meet his/her desired waveform requirements.

2.3. FPGA Design

The FPGA logic consists of ADC controller, data receiving module, frequency measurement module, etc., where the ADC controller and frequency measurement module need to be realized by using the FPGA built-in counter and clock module; the data receiving module is used to receive and store the data streams from the ADC and to perform the processing, such as data sampling.

2.3.1. Data Acquisition Design

The analog signal is acquired by the ADC, which has a sampling frequency of 1 GHz and an FPGA system clock of 250 MHz. to ensure synchronization and avoid substability problems, we add a FIFO to the process. this FIFO is used to synchronize the ADC data with the system clock for subsequent processing. the width of the FIFO is 64 bits, the depth is 15, and its output logic is to write 64-bit data in each clock cycle and read 64-bit data in the next clock cycle to realize data buffering. The data size of each channel is 32 bits, and the 64-bit data contains the data of two ADC channels. Considering that the ADC chip has 8 bits, the 32-bit data for each channel contains 4 sample signals, The data acquisition design RTL diagram is shown in Figure 2.

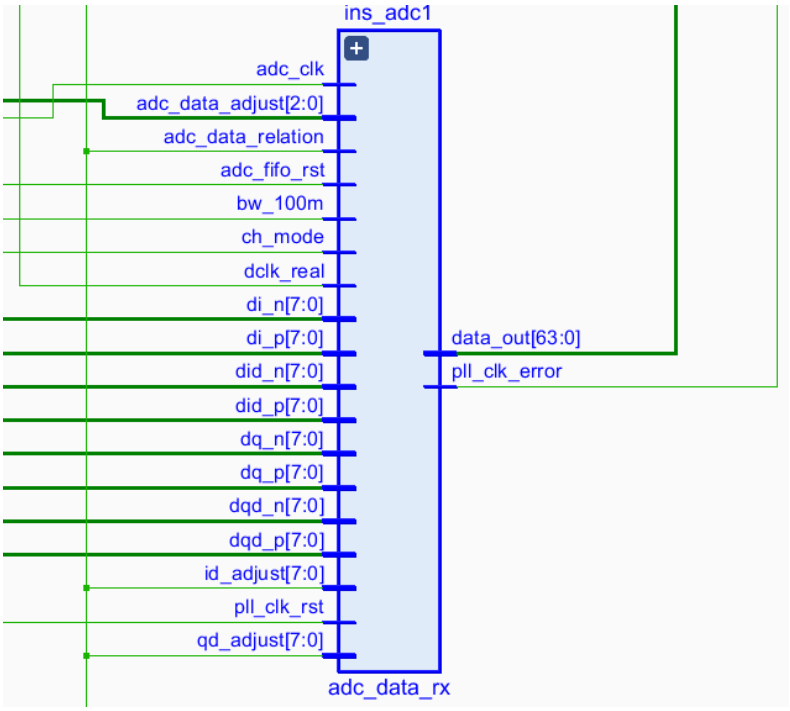

Figure 2. Data Acquisition RTL Diagram

2.3.2. Frequency Measurement Module Design

In this design, frequency measurement is performed by counting the rising edge of the input signal after comparison for a fixed time [9], and the frequency value is calculated as the count value divided by the fixed time. Since the input signal is sinusoidal, the acquired signal needs to be converted to a square wave signal. In this design, every 8 bits of the 32-bit data are extracted and a Schmitt comparison is performed and the result is deposited into a 4-bit signal. By comparing two data with the same 4-bit signal, we can obtain the rising edge of the data and count the number of "1s" stored in the 4-bit register. The Schmitt trigger compares the upper 8 bits of the input signal, the signal exceeding the upper limit is recorded as 1, the signal exceeding the lower limit is recorded as 0, and the signal kept between the upper and lower limits remains in its original state. The measurement range of this method is 0-500M and the error is within 10 cycles,The frequency measurement module RTL diagram is shown in Figure 3.

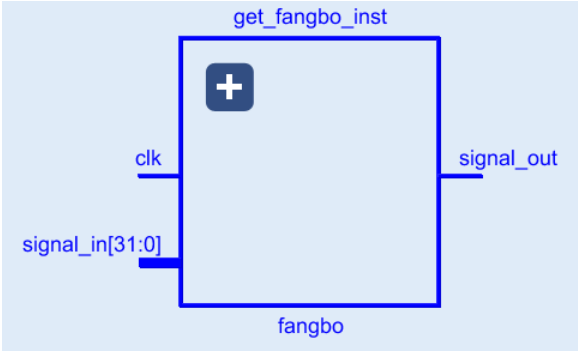

Figure 3. The frequency measurement module RTL diagram

2.3.3. Pumping Point Module Design

In this design, the pumping point module adopts the method of equal interval pumping point. The idea is to select the number of times of extraction according to the frequency of measurement, and write the data into FIFO by controlling the number of times of extraction [10].The module can select different extraction methods according to the input D_model, including 1 times extraction, 2 times extraction and N times extraction. The extracted data is output through data_out, where wr_en indicates whether the extracted data is written to FIFO or not, The pumping point module RTL diagram is shown in Figure 4.

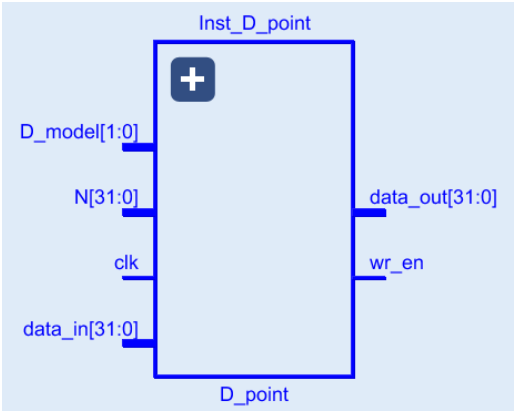

Figure 4. The pumping point module RTL diagram

2.3.4. Data Transmission Design

The data transfer design RTL diagram is shown in Figure 5.

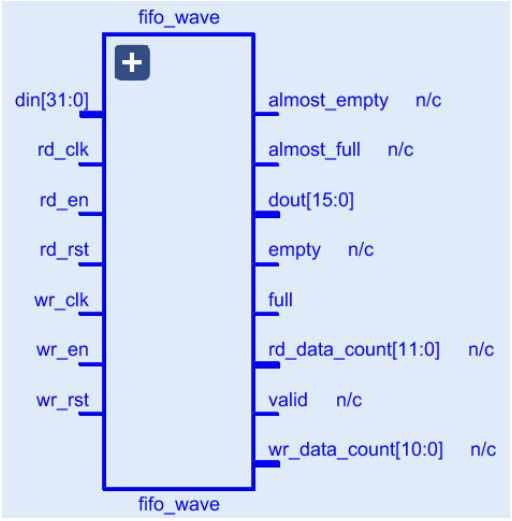

Figure 5. The data transfer design RTL diagram

After signal reception, shaping, frequency measurement and pumping point processing, the processed signal will be stored into the FIFO. Since the FPGA to ARM bus is 16-bit, the write depth of the FIFO is set to 2048 with a width of 32 bits; the read depth is set to 4096 with a width of 16 bits. At the same time, the data address and full address of the FIFO are corresponded to the ARM address to wait for the ARM read signal.

3. RESULT TEST

After the completion of the design of the oscilloscope overall function test, the basic function test content is as follows: can realize the measured signal data acquisition and storage, sampling rate of 1GSPS, input bandwidth of 200MHz, and can realize the oscilloscope's time base, amplitude, and triggering and automatic test function.

3.1. Signal Acquisition Test

For the input signal test, to see if the oscilloscope can acquire and store signals, and the input bandwidth is 200 M. The test method is to observe the screen display waveforms and the peak-to-peak value of the waveforms displayed against the oscilloscope to see if they are consistent. 200 M input signal test results are shown in Figure 6.

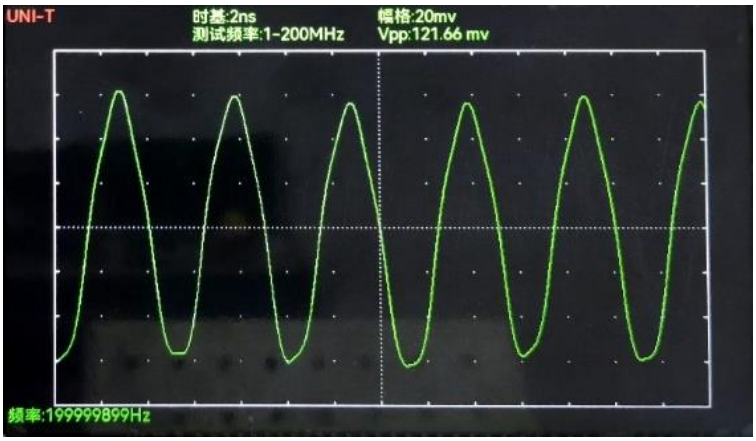

Figure 6. 200M Test Signal Results

The input signal amplitude is 120mv, the frequency is 200MHz, as can be seen in Figure 6, after the oscilloscope shows the signal peak-to-peak value of 121.6mv, the frequency is 1999999899Hz, and the input signal results are close to the oscilloscope can be verified that the oscilloscope's bandwidth of 200M indicators.

3.2. Time, Amplitude and Trigger Function Test

Acquire the signal and wait until the signal is stable to observe the number of horizontal grid points occupied by the signal for one cycle and the time base corresponding to the number of horizontal grid points to calculate the signal frequency to see if it corresponds to the initial frequency to verify whether the time base function is correct; acquire the signal and wait until the signal is stable to observe the number of vertical grid points occupied by the signal for one cycle and the amplitude corresponding to the number of vertical grid points to calculate the signal peak-to-peak value to verify whether the amplitude function is correct; acquire the signal and observe whether the waveform is jittery or not, with or without ghosting to verify whether the trigger function is correct. Observe whether the waveform is jittery, with or without ghosting can verify whether the trigger function is correct or not, the results of the three major function tests are shown in Figure 7.

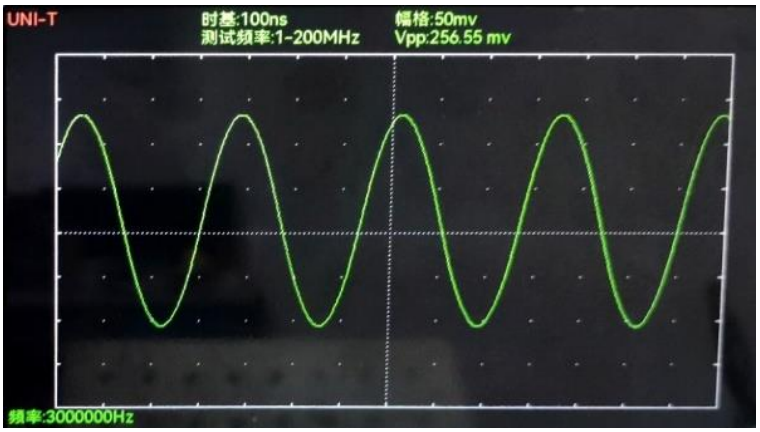

Figure 7. Basic Functional Test Diagram

Figure 7, the input signal frequency of 3MHz, amplitude peak value of 256mv, at this time, the oscilloscope waveform interface horizontal grid point a occupancy time of 100ns, longitudinal grid point a grid amplitude of 50mv, from the naked eye can be observed, the waveform occupies the horizontal grid point of 3.3 grid, longitudinal grid point occupies the 5 grids, with the theoretical value of wanting to be close to the waveform, and the waveform is not ghosting, jitter phenomenon, it can be verified that the design of this The correctness of the time base, amplitude and trigger function can be verified.

3.3. Automatic Function Test

Use the key to adjust the original waveform at will, and then press the trigger button to observe the oscilloscope phenomenon and use the cell phone stopwatch for timing, the automatic function test results are shown in Figure 8.

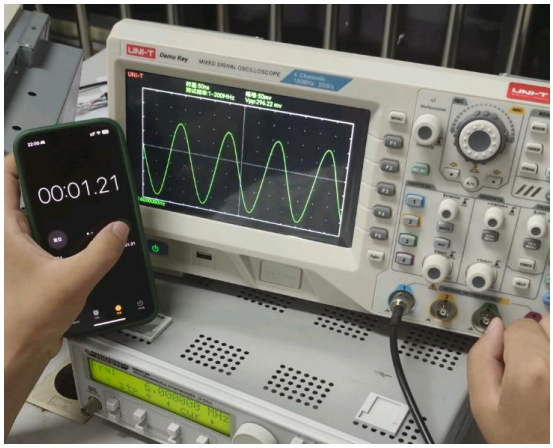

Figure 8 Automated Functional Test Diagram

From Figure 8, it can be seen that the time spent after pressing the auto button is 1.21 seconds, and the waveform occupies a suitable position on the screen, which can verify the correctness of the auto function of this design.

3.4. Indicator Satisfaction

As a result of the above tests, all tests were summarized in this section and the summary table is shown in Table 1.

Table 1. Three Scheme comparing

Number	Test Items	Technical Indicators	Satisfaction
1	Bandwidth	200M	Satisfaction of design indicators
2	Time base	Waveforms occupy a small time base with actual error	Satisfaction of design indicators
3	Amplitude	Small error between the amplitude of the waveform and the actual error.	Satisfaction of design indicators
4	Trigger Function	Stable waveform without ghosting	Satisfaction of design indicators
5	Auto Function	Screen display 3-5 cycles, 60% of the vertical frame	Satisfaction of design indicators

4. CONCLUSION

This paper implements the three basic functions of the oscilloscope: time base, amplitude and trigger, and optimizes the automatic trigger function on the basis of its implementation, including FPGA design and ARM design. The feasibility and accuracy of the oscilloscope is proved by testing and verifying the acquisition and storage function, time base amplitude control and automatic setting function of the oscilloscope.

In the future, the performance of oscilloscopes can be further optimized and improved to cope with increasingly complex test environments and special test objects. At the same time, more advanced artificial intelligence algorithms and technologies can be explored to improve the identification and capture of abnormal signals and achieve more accurate test results. In addition, combined with cloud computing and IoT and other technologies, a more intelligent and remotely manageable test system can be constructed to improve test efficiency and convenience. Overall, with the continuous development of the electronics industry, test instruments will continue to evolve to provide stronger support for the development of the industry.

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